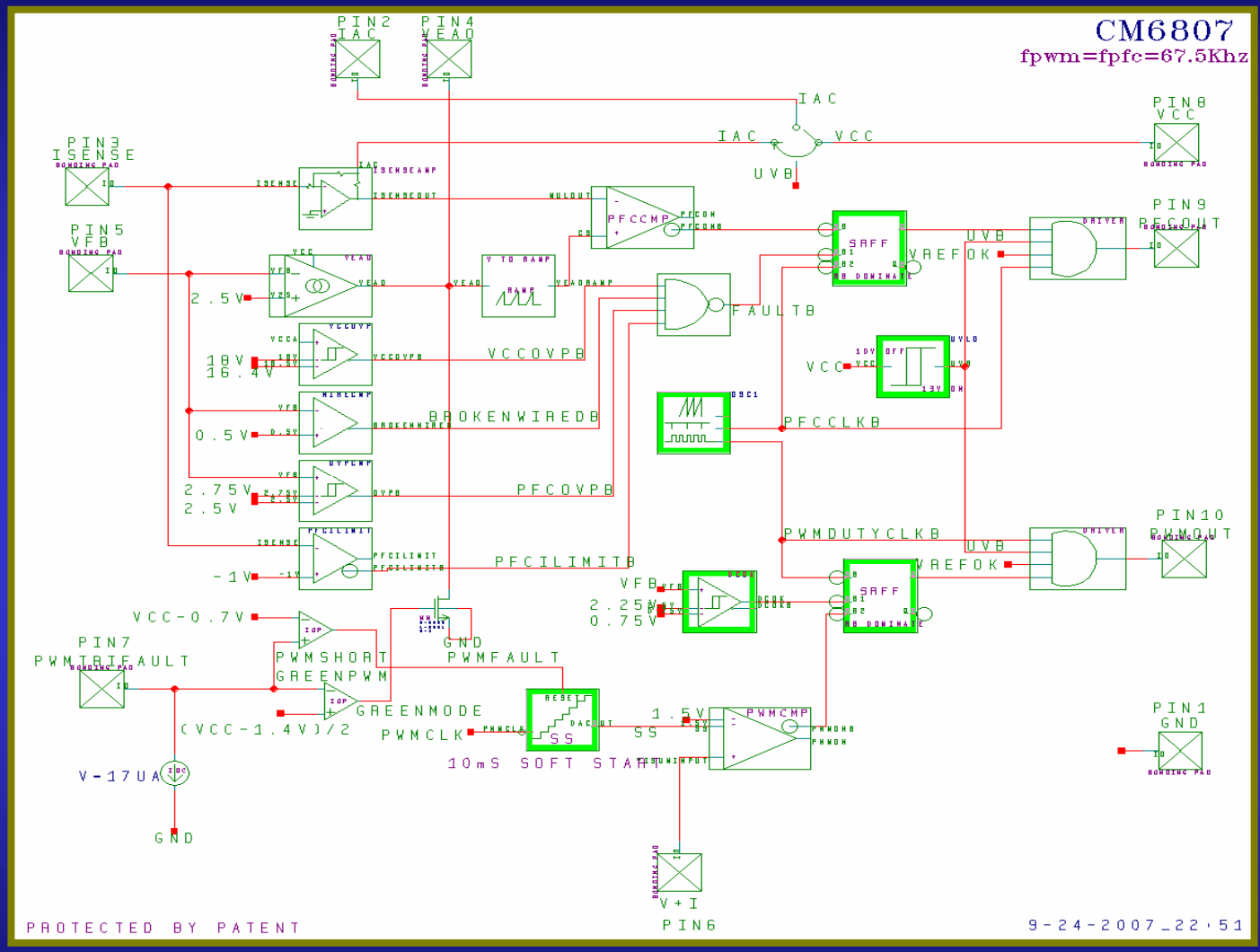
PFC + Stand By
CM6807

85+
with
10 pin PFC/Stand By
Combo

CM6807

Design process



CM6807
Simplified Block Diagram

PFC Control:

Leading Edge Modulation with Input Current Shaping Technique

(ICST)

PFC Control: ICST

- ICST is based on the following equations:

$$R_e = V_{in} / I_{in} \qquad (1)$$

$$\bar{I}_l = I_{in} \qquad (2)$$

- Equation 2 means: average boost inductor current equals to input current.
- Assume that input instantaneous power is about to equal to the output instantaneous power.

$$\therefore V_{in} \times \bar{I}_l \approx V_{out} \times \bar{I}_d \qquad (3)$$

$$V_{out} / V_{in} = 1 / (1 - d) \qquad (4)$$

- For steady state and for the each phase angle, boost converter DC equation at continuous conduction mode is:

•Rearrange above equations, (1), (2),(3), and (4) in term of Vout and d, boost converter duty cycle and we can get average boost diode current equation (5):

$$\bar{I}_d = (1-d)^2 \times V_{out} / R_e \qquad (5)$$

•Also, the average diode current can be expressed as:

$$\bar{I}_d = \frac{1}{T_{sw}} \int_0^{T_{off}} I_d(t) \cdot dt \qquad (6)$$

•If the value of the boost inductor is large enough, we can assume

$$I_d(t) \sim I_d$$

I_d is constant during each switching period, 1/67.5khz.

•It means during each cycle or we can say during the sampling, the diode current is a constant.

•Therefore, equation (6) becomes:

$$\bar{I}_d = {I_d \times t_{off}}/{T_{sw}} = I_d \times d' = I_d \times (1-d)$$

(7)

$$I_d \times d' = (d')^2 \times V_{out} / R_e$$

$$\therefore I_d = d' \times V_{out} / R_e$$

$$\therefore I_d = \frac{V_{out}}{R_e} \times \frac{t_{off}}{T_{sw}} \quad (8)$$

•Using this simple equation (8), we implement the PFC control section of the PFC-PWM controller, CM6805/6 & CM6903

Review Leading Edge Modulation & Average Current Mode PFC Control

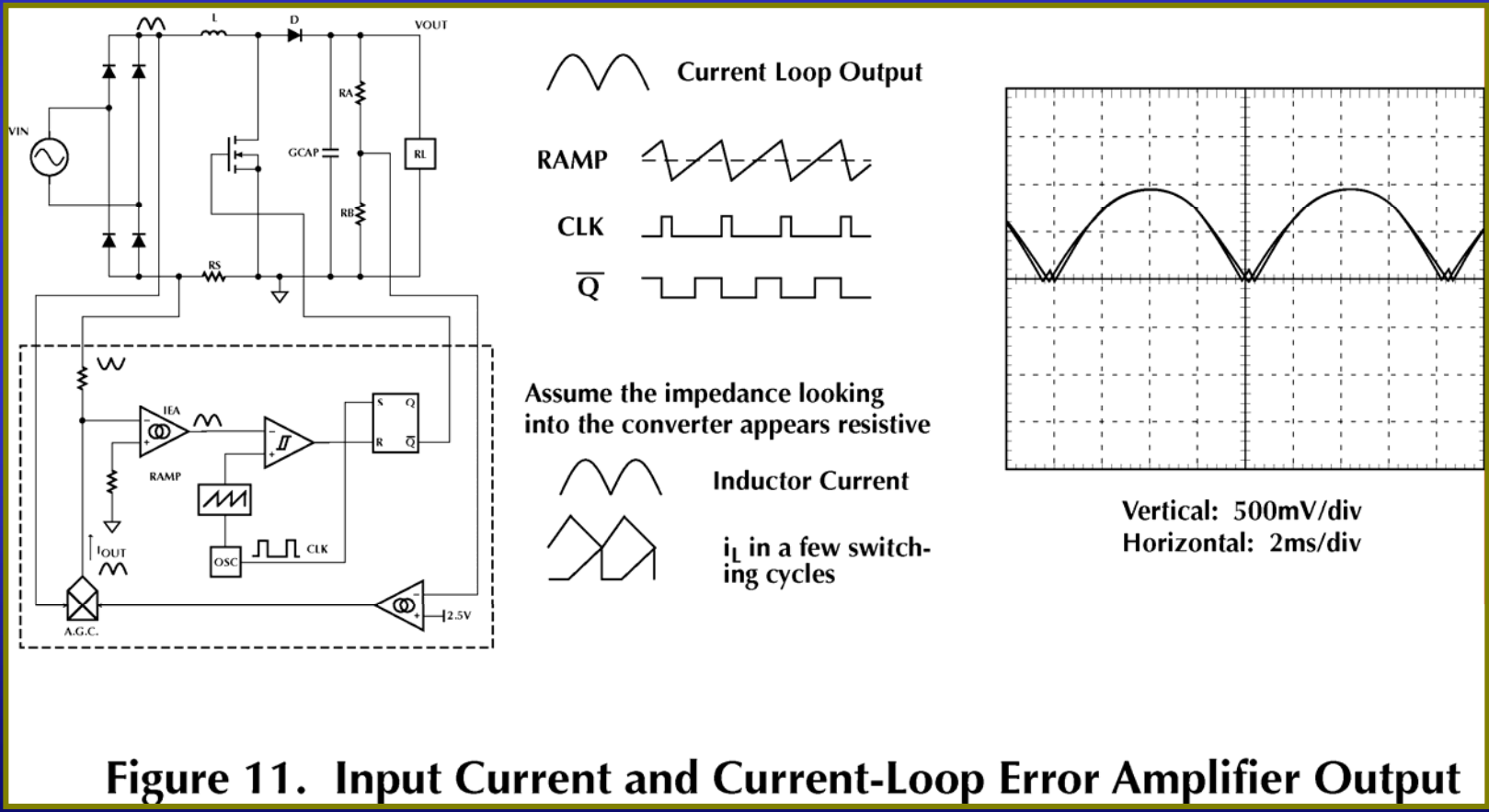
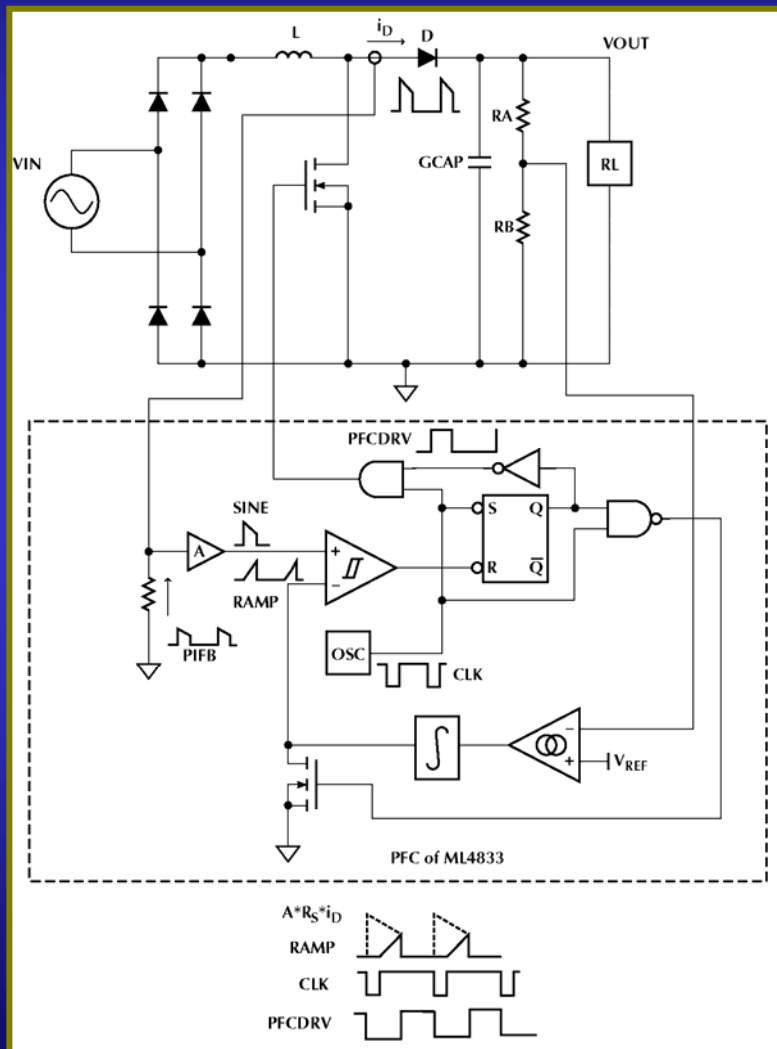


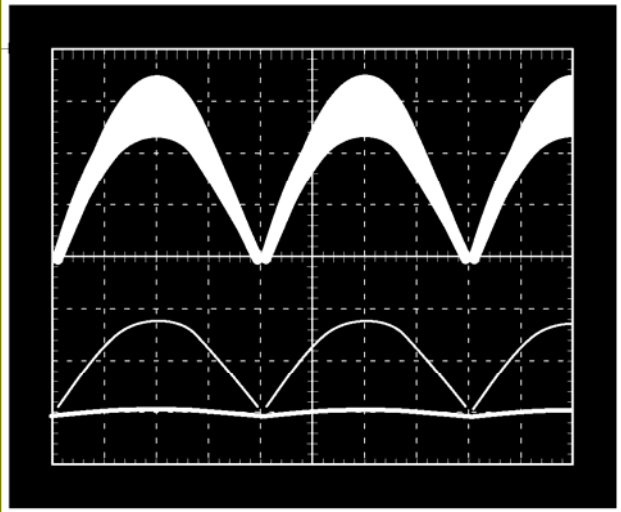
Figure 11. Input Current and Current-Loop Error Amplifier Output



- Sensing diode current (can use either current sense transformer for efficiency or simple current sense transistor)
- No AGC or multiplier
- Easy to compensate
- Automatic slope compensation
- AC or DC input

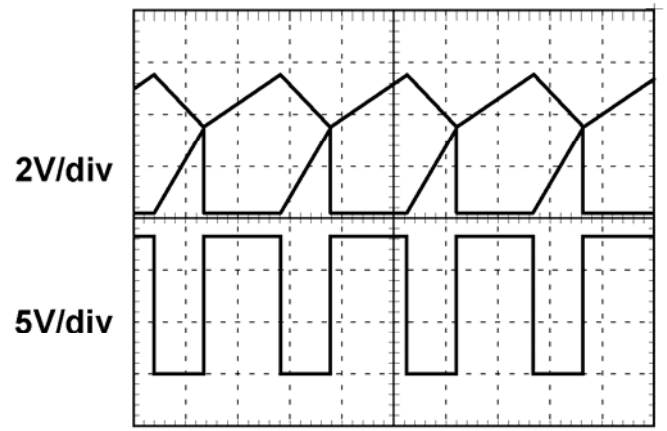
Figure 12a. Input Current Shaping PFC Control

Experimental Results of 100W Boost Converter

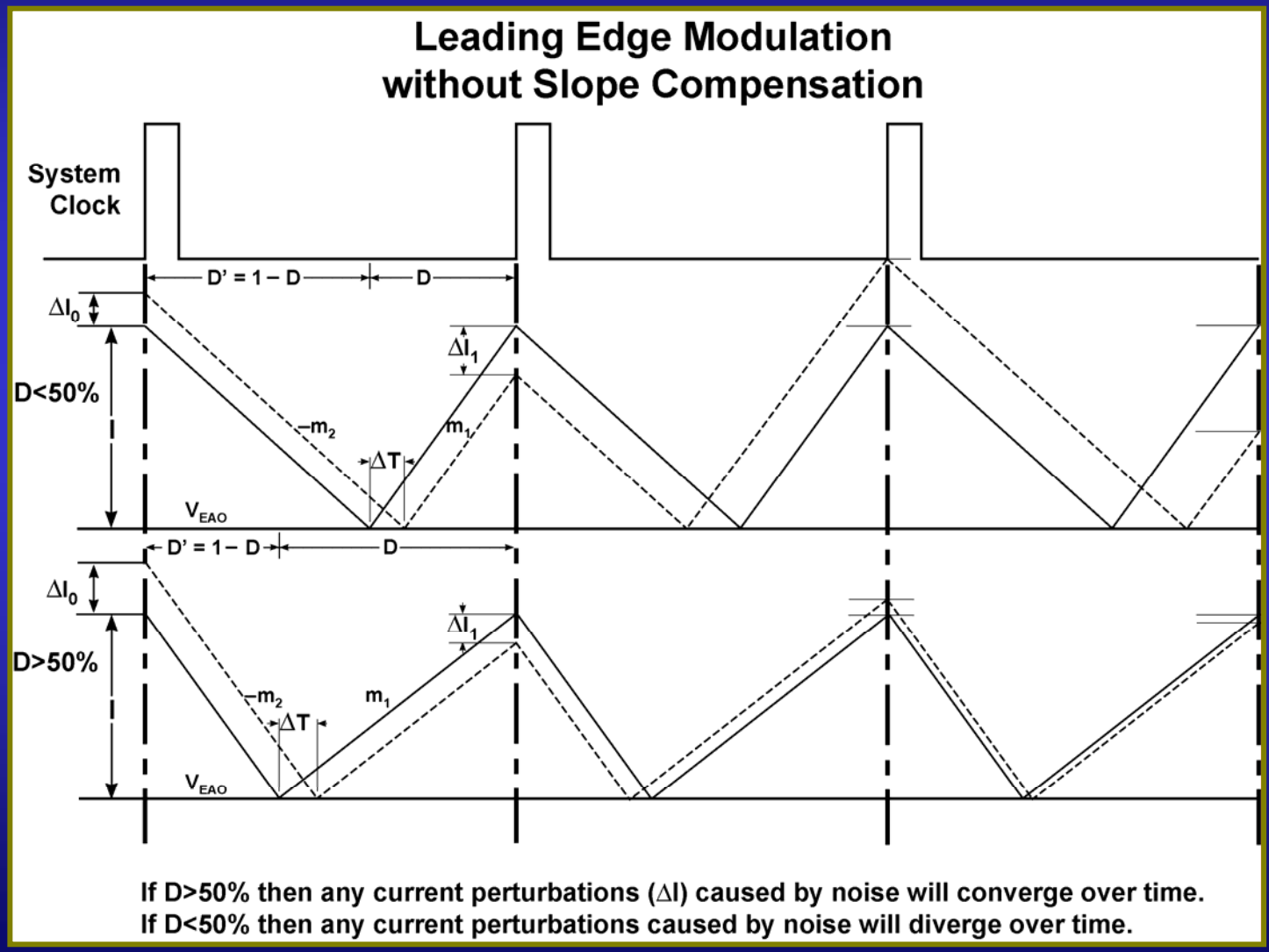


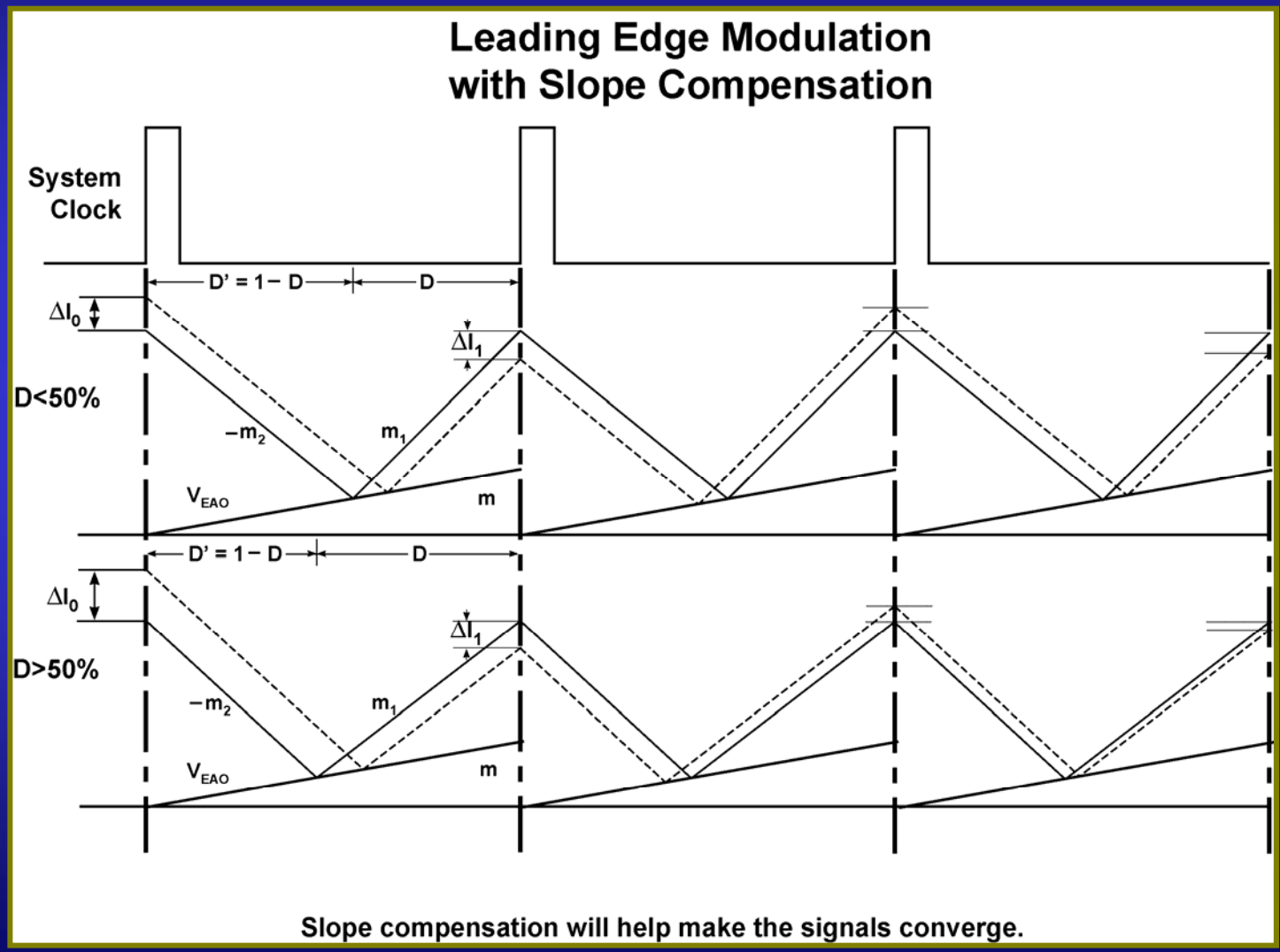
Top Trace: Voltage Signal of Inductor Current
Bottom Trace: RAMP

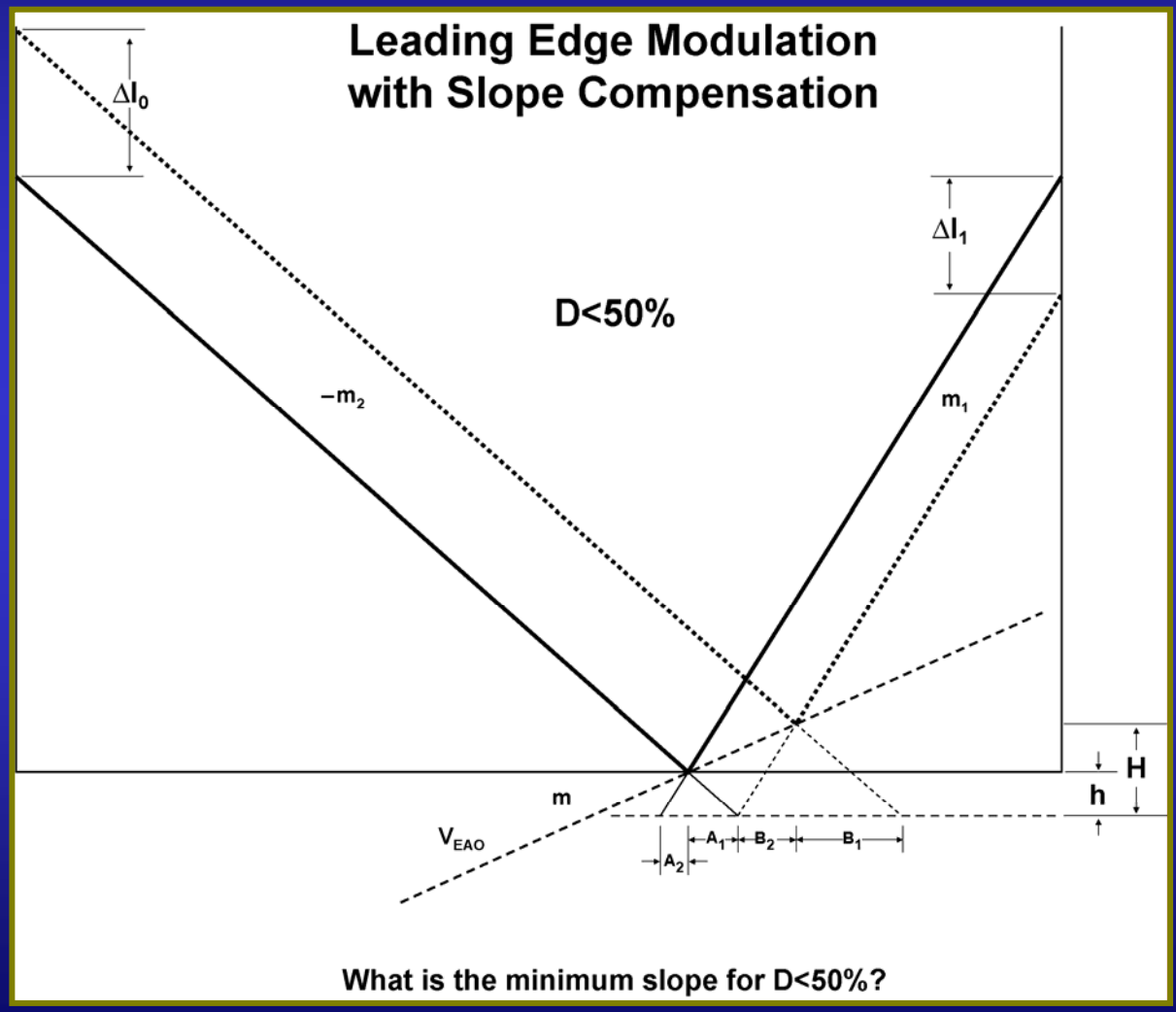
Duty Cycle Timing

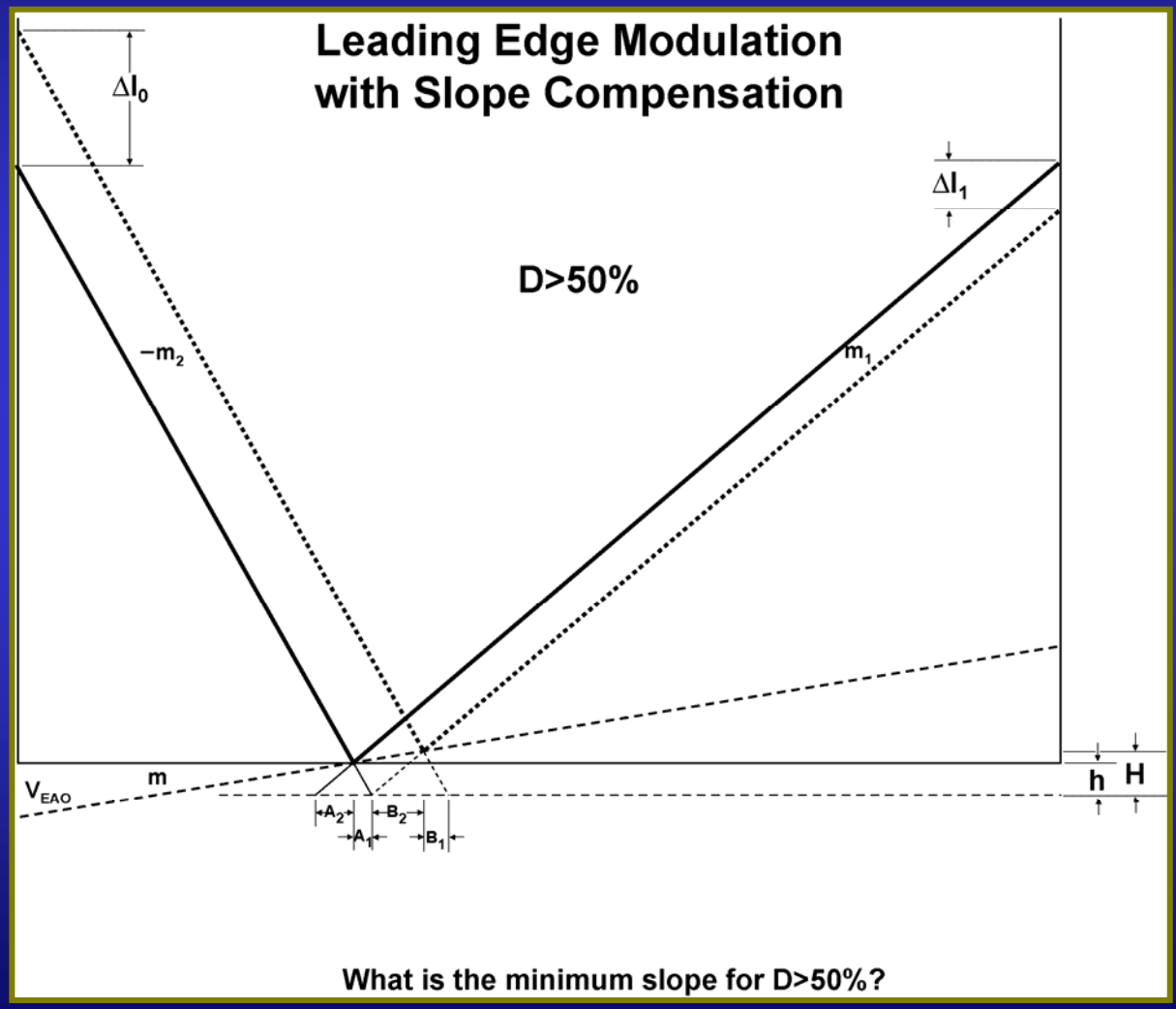


Top Trace: Voltage Signal of Inductor Current
Middle Trace: RAMP
Bottom Trace: PFC Gate Drive

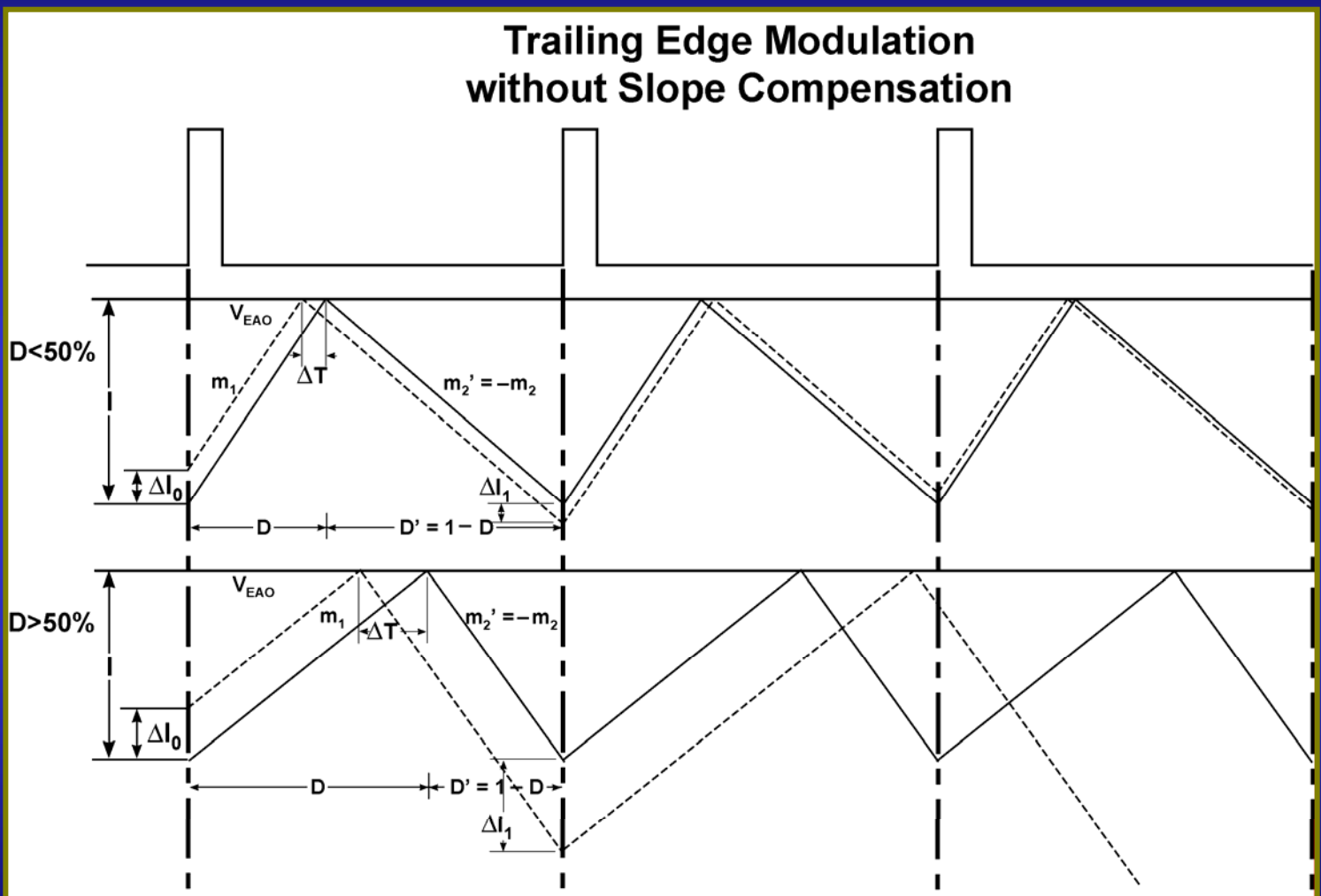

Leading Edge Modulation
without Slope Compensation
System Clock
D' = 1 – D
D
ΔI0
ΔI1
D<50%
–m2
m1
ΔT
VEAO
D' = 1 – D
D
ΔI0
ΔI1
D>50%
–m2
m1
ΔT
VEAO
If D>50% then any current perturbations (ΔI) caused by noise will converge over time.
If D<50% then any current perturbations caused by noise will diverge over time.


Leading Edge Modulation
with Slope Compensation
System
Clock
D' = 1 – D
D
ΔI0
ΔI1
D<50%
–m2
m1
VEAO
m
D' = 1 – D
D
ΔI0
ΔI1
D>50%
–m2
m1
VEAO
m
Slope compensation will help make the signals converge.


Leading Edge Modulation
with Slope Compensation
ΔI0
ΔI1
D<50%
−m2
m1
m
VEAO
A2
A1
B2
B1
H
h
What is the minimum slope for D<50%?

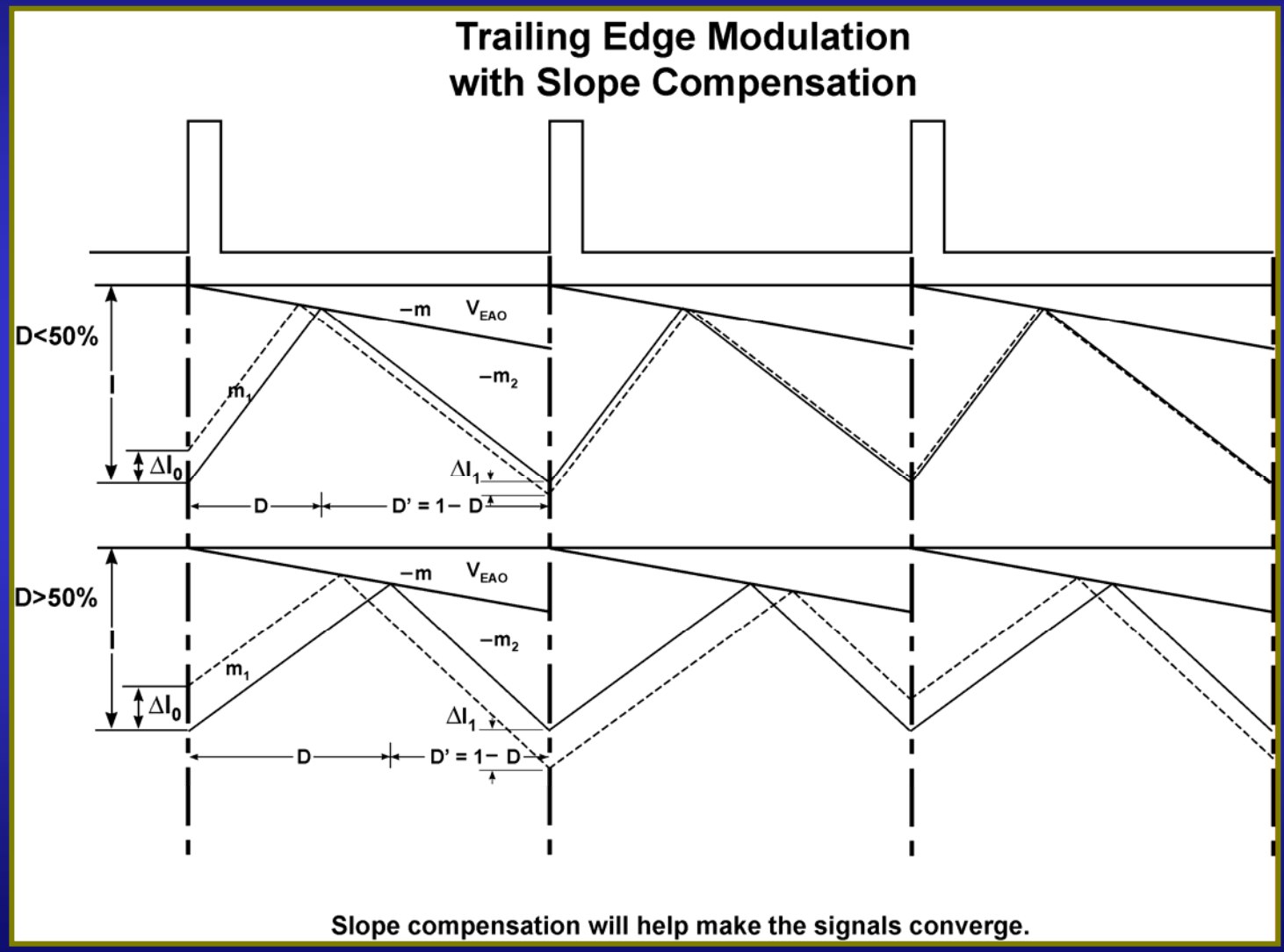

Leading Edge Modulation
with Slope Compensation
ΔI0
ΔI1
D>50%
−m2
m1
VEAO
m
A2
A1
B2
B1
h
H
What is the minimum slope for D>50%?

Trailing Edge Modulation without Slope Compensation



If D<50% then any current perturbations (ΔI) caused by noise will converge over time.
If D>50% then any current perturbations caused by noise will diverge over time.

PFC Control: ICST



Leading edge modulation current-mode needs slope compensation when D (the duty cycle) <0.5.

V_{EAO} is the voltage error amplifier output;
I is the inductor current;
m_1 is the rising slope of the inductor current waveform;
m_2 is the falling slope of the inductor current waveform.

The following equations can be derived:

$$\Delta T = \frac{\Delta I_0}{m_2} \qquad (1)$$

$$\Delta T = \frac{\Delta I_1}{m_1} \qquad (2)$$

(1) and (2) yield (3):

$$\Delta I_1 = -\Delta I_0 \times \frac{m_1}{m_2} \qquad (3)$$

In general form:

$$\Delta I_n = \left(-\Delta I_0 \times \frac{m_1}{m_2}\right)^n \qquad (4)$$

$$D' = 1 - D \qquad (5)$$

$$I = m_2 \times D' \qquad (6)$$

$$I = m_1 \times D \qquad (7)$$

$$m_2 \times D' = m_1 \times D \qquad (8)$$

So the relationship between D and ΔI is:

$$\Delta I_n = \left(-\Delta I_0 \times \frac{D'}{D}\right)^n \qquad (9)$$

This leads to the conclusion that when the duty cycle (D) is greater than 50% for leading edge modulation without slope compensation the current loop is stable. And, when the duty cycle is less than 50%, the current loop is unstable.
When a current-mode converter uses leading edge modulation with slope compensation the current loop is stable for all values of duty cycle.

In the next set of equations A, A_1, A_2, B, B_1, B_2, H, and h are used for deriving the equations and have no physical properties.

$$A = \frac{\Delta I_1}{m_1} \qquad A_1 = \frac{h}{m_2} \qquad A_2 = \frac{h}{m_1}$$

$$B = \frac{\Delta I_0}{m_2} \qquad B_1 = \frac{H}{m_2} \qquad B_2 = \frac{H}{m_1}$$

$$A = A_1 + A_2 \qquad B = B_1 + B_2 \qquad H - h = (A_1 + B_2) \times m$$

From these the relationships among the inductor current slopes, the compensation slope, and the inductor current difference are:

$$\Delta I_1 = -\Delta I_0 \times \frac{(m_1 - m)}{(m_2 + m)} \qquad (10)$$

For a stable current loop the following equations exist:

$$\frac{(m_1 - m)}{(m_2 + m)} < 1 \qquad (11) \qquad m > 0.5 \times m_1 \qquad (12)$$

PFC Current Mode Leading Edge Modulation:

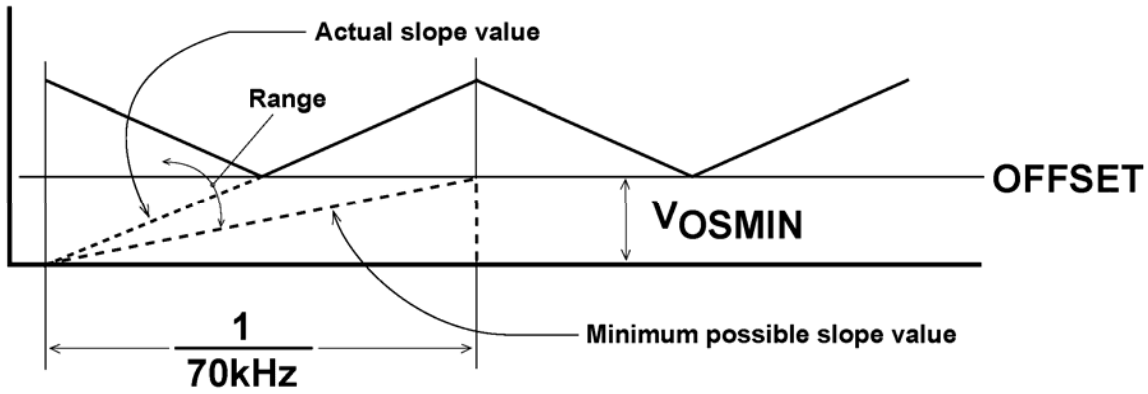
When Duty Cycle is less than 50%, it needs the slope compensation.
Vos goes up <-----> Ramp Slope goes up

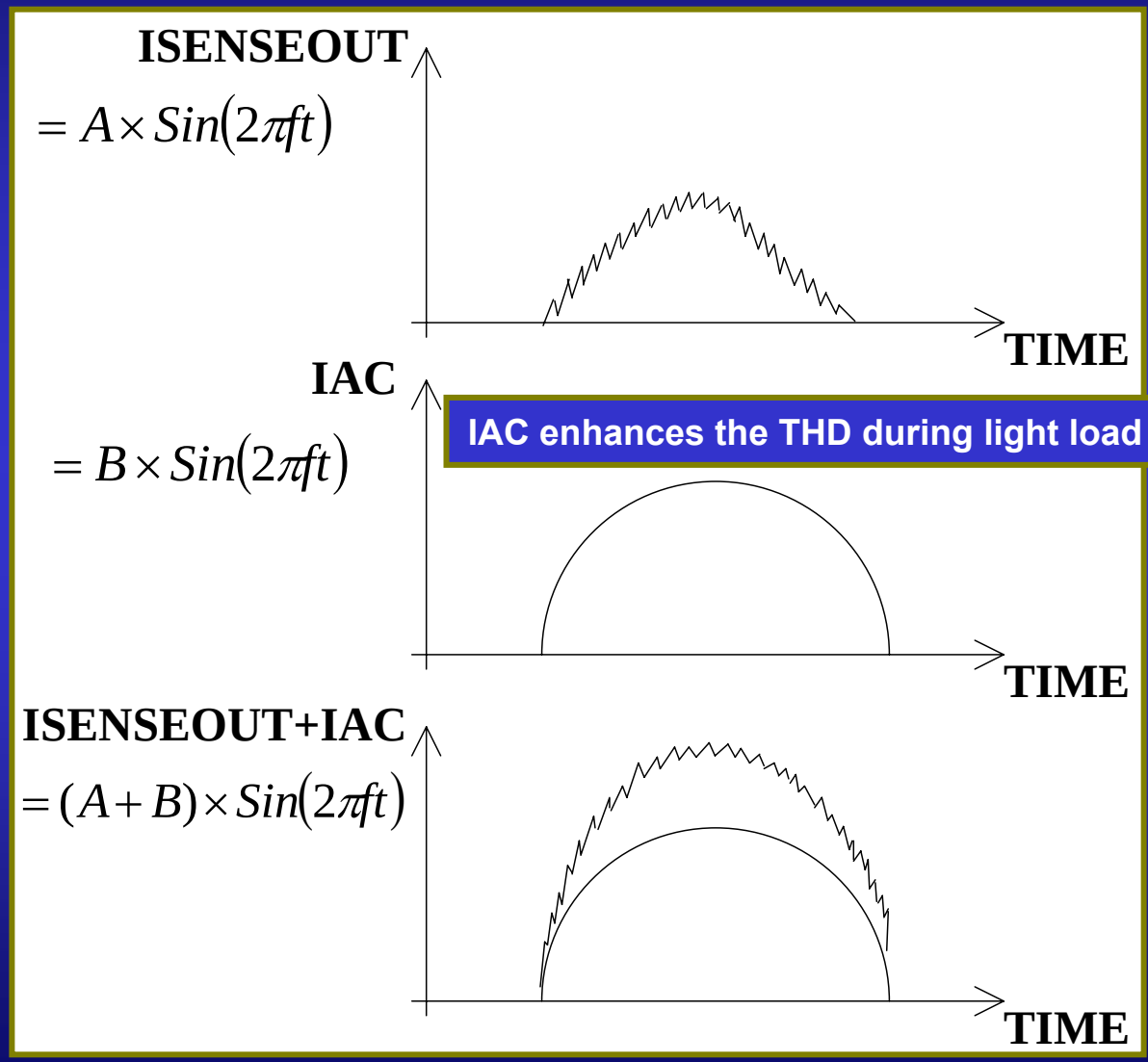
The worst condition occurs when D = 0 and V_{IN} = 380V.
At that time:

$$\frac{di_L}{dt} = \frac{V_{IN}}{L} = \frac{380}{L} \quad (1)$$

$$\frac{1}{S \times R_{Filter} \times C_{Filter} + 1} \times R5 \times \frac{di_L}{dt} = \frac{380}{L} \times R5 \times \frac{1}{S \times R_{Filter} \times C_{Filter} + 1} \quad (2)$$

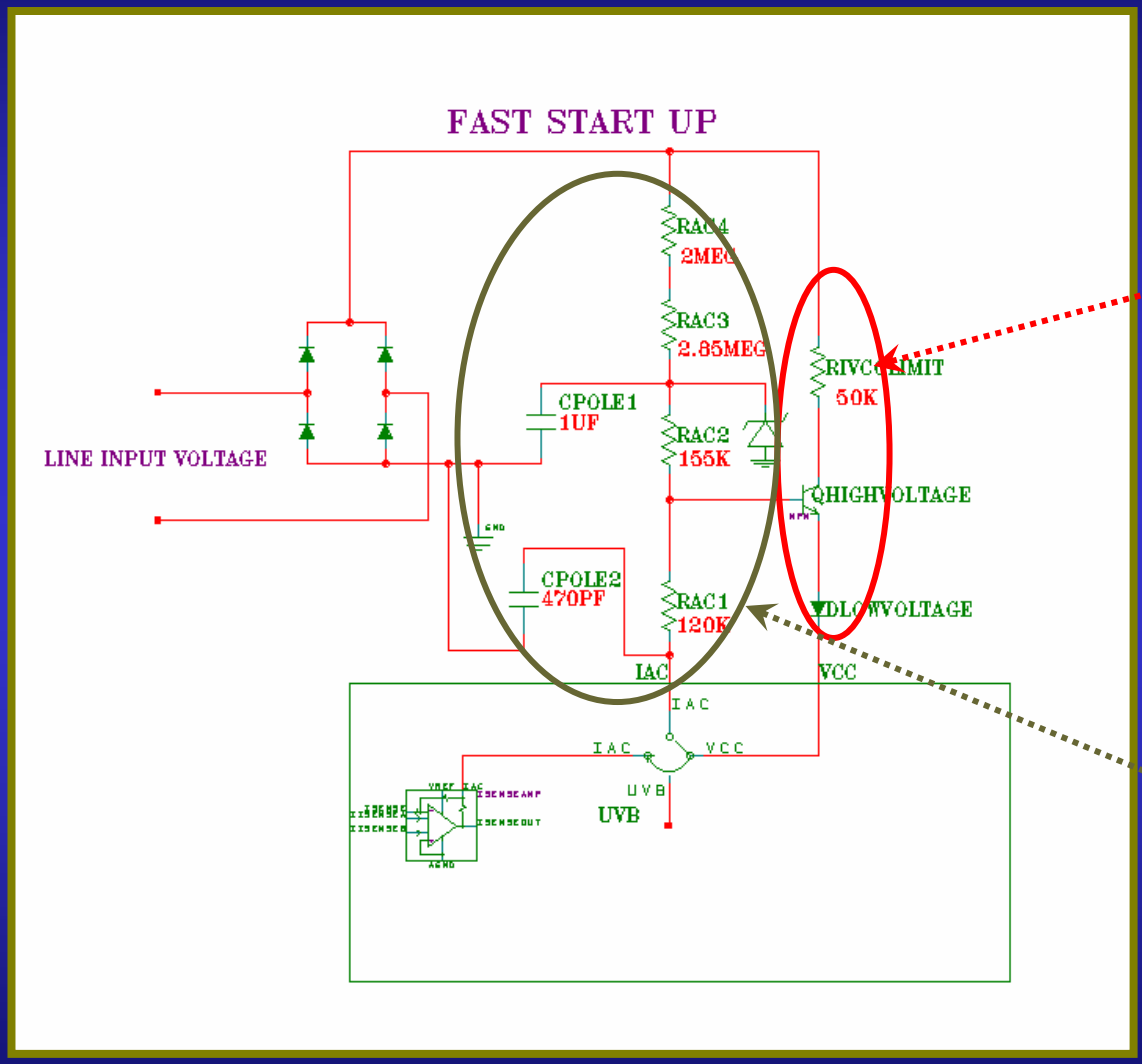
$$\therefore V_{OSMIN} = \frac{380}{L} \times R5 \times \frac{1}{\sqrt{(R_{Filter} \times C_{Filter} \times 2\pi 70kHz)^2 + 1^2}} \times \frac{1}{70kHz} \quad (3)$$




ISENSEOUT
$= A \times Sin(2\pi ft)$
TIME
IAC
$= B \times Sin(2\pi ft)$
IAC enhances the THD during light load and high line
TIME
ISENSEOUT+IAC
$= (A+B) \times Sin(2\pi ft)$
TIME

IAC, Pin 2: StartUp and PFC Slope Comp
VCC, Pin 8 For fast start up applications

PFC Control: ICST



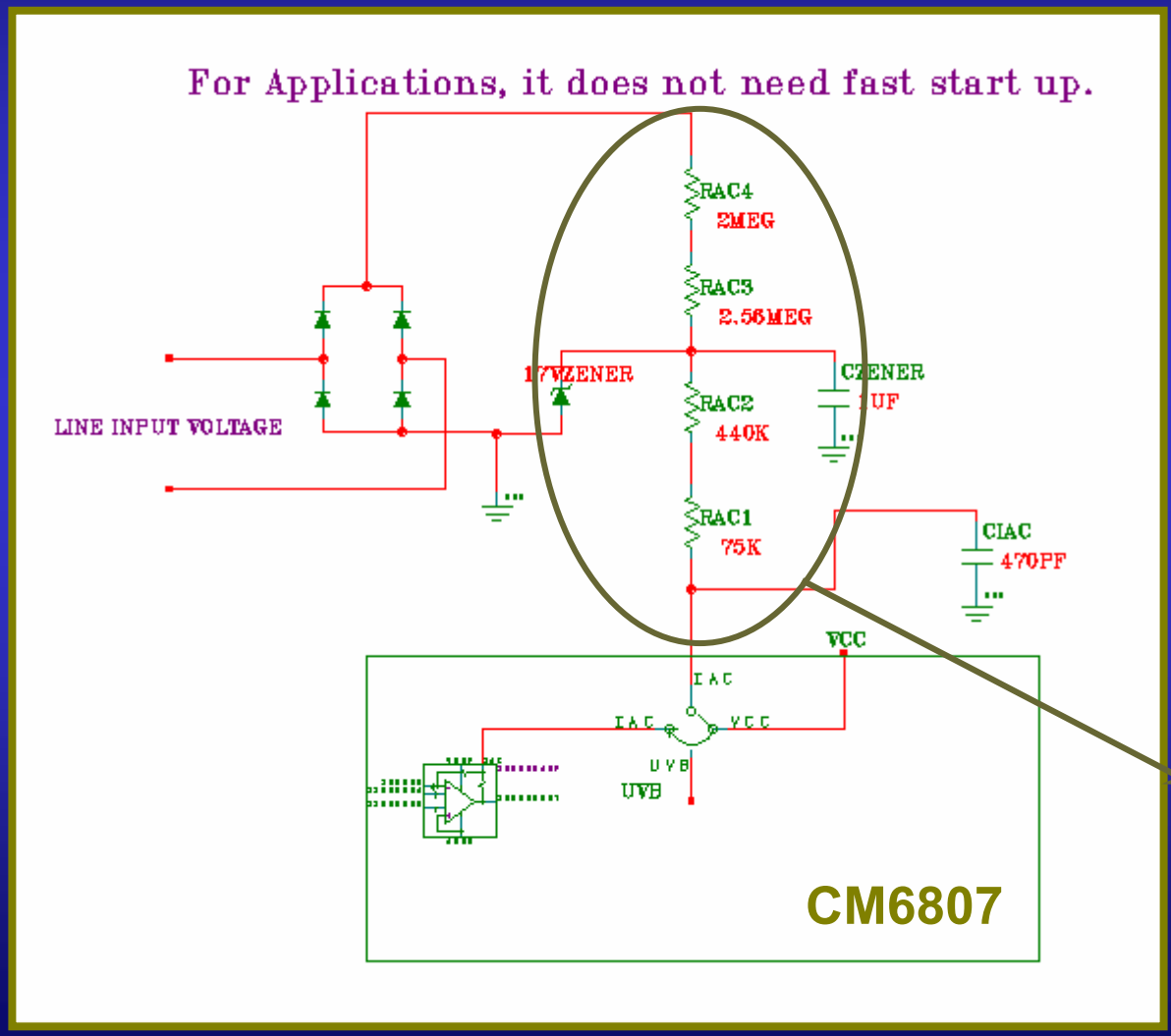
Vcc Fast Start Up
$I_{cc\ start\ up}$ typical~100uA

PFC Current Loop Slope Compensation

CM6807 IAC have the Switch to switch to VCC During start up

IAC, Pin 2: StartUp and PFC Slope Comp
VCC, Pin 8

PFC Control: ICST



PFC Current Loop
Slope Compensation

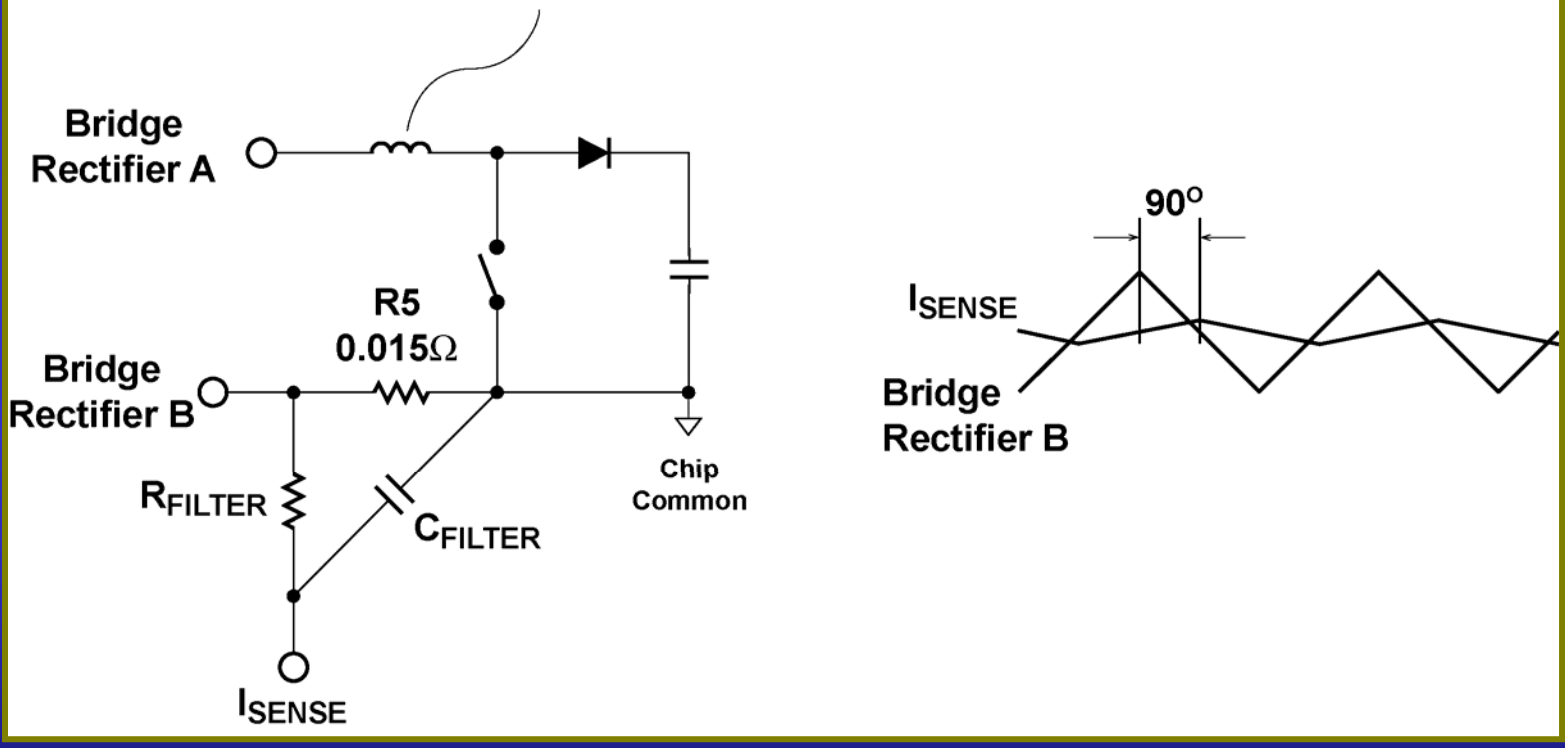
PFC Control: ICST

Isense, Pin 3

2 purposes to add Isense filter:

- Protect IC during inrush current
- Using smaller inductor and still having good THD

To Reduce Boost Inductor

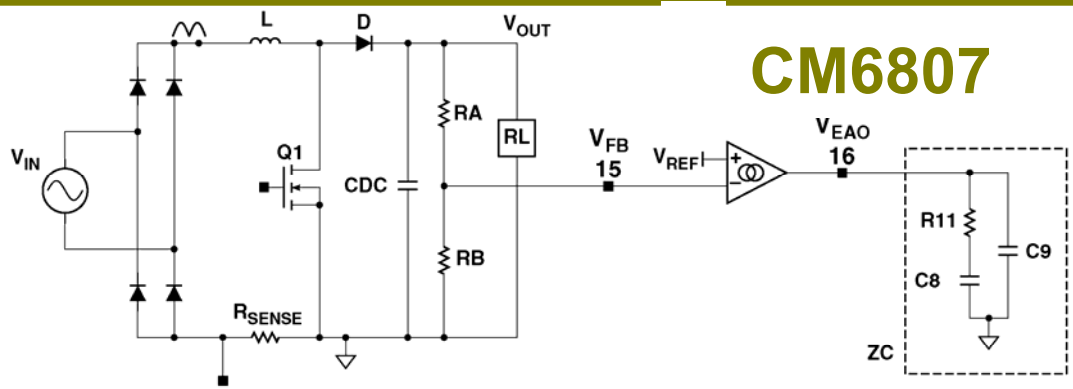


Usually, the pole of Isense filter ~ 1/6 of the switching frequency, and it is $fsw/6 = 1/(2 \times \pi \times R_{filter} \times C_{filter})$

If R_{filter} =1K Ω, C_{filter} =14.15nF.

Veao (pin4) and Vfb (pin5)

PFC Control: ICST



$$\because \frac{\Delta V_{OUT}}{\Delta V_{EAO}} = \frac{P_{IN\ AVERAGE}}{V_{OUT} \times \Delta V_{EAO} \times S \times C_{DC}} \quad (1)$$

$$\because \frac{\Delta V_{FB}}{\Delta V_{OUT}} = \frac{R_B}{R_A + R_B} = \frac{2.5V}{380V} \quad (2)$$

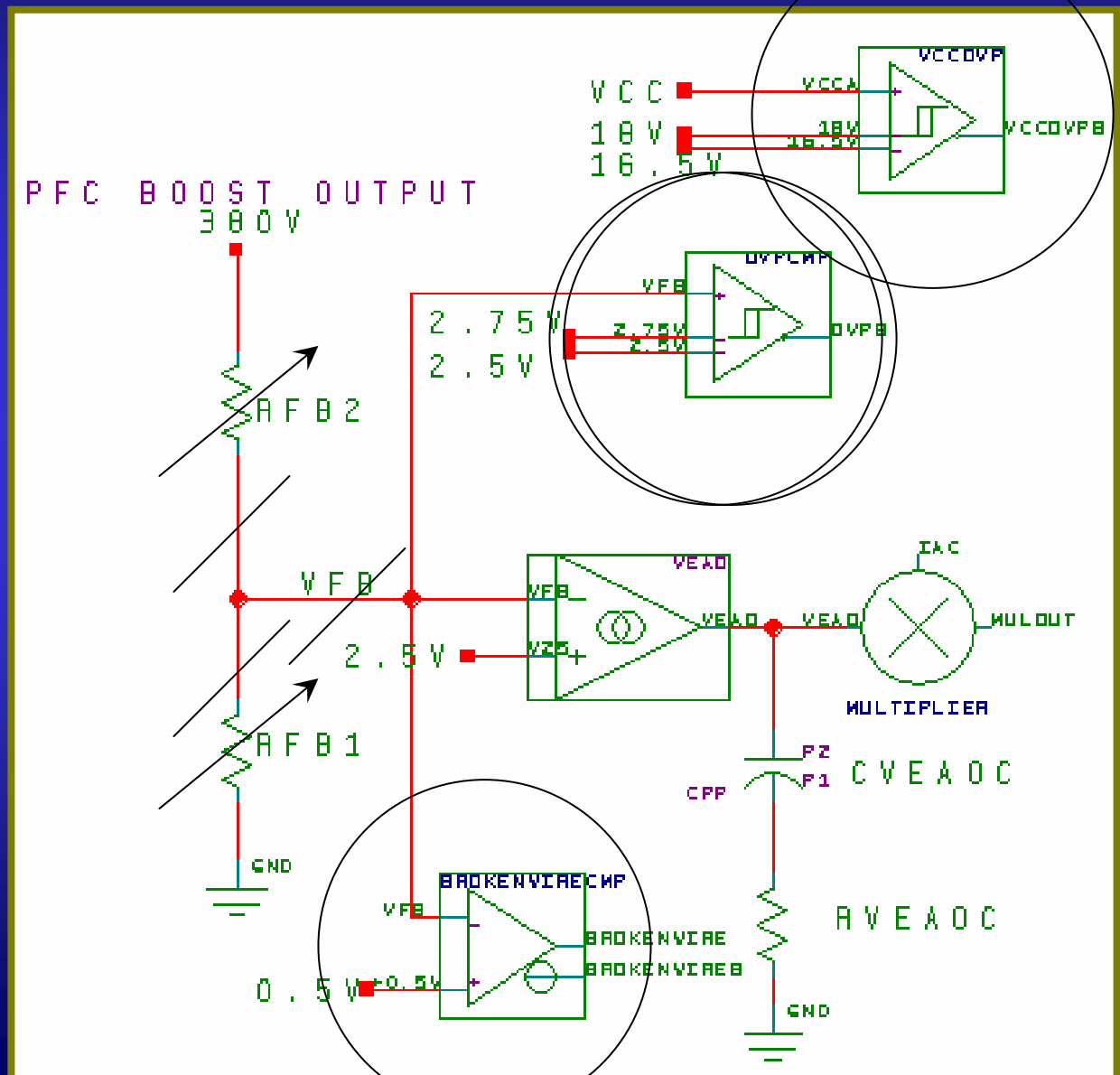
$$\because \frac{\Delta V_{EAO}}{\Delta V_{FB}} = Gm \times Z_C \quad (3)$$

$$\therefore \text{Loop Gain} = \frac{\Delta V_{OUT}}{\Delta V_{EAO}} \times \frac{\Delta V_{FB}}{\Delta V_{OUT}} \times \frac{\Delta V_{EAO}}{\Delta V_{FB}} = \frac{P_{IN\ AVERAGE} \times 2.5V}{V_{OUT} \times \Delta V_{EAO} \times S \times C_{DC} \times 380V} \times Gm \times Z_C \quad (4)$$

For CM6807,
ΔV_{EAO}~ 6V - 0.7V = 5.3V

Veao (pin4) and Vfb (pin5)

PFC Control: ICST



Easy to meet UL1950

GND (pin1)

Layout Issues, in order of importance

#1: R5 and R11 must be physically butted against one another, and their junction must be connected to the IC Ground pin. If there is switching current minimize the distance to chip gnd.

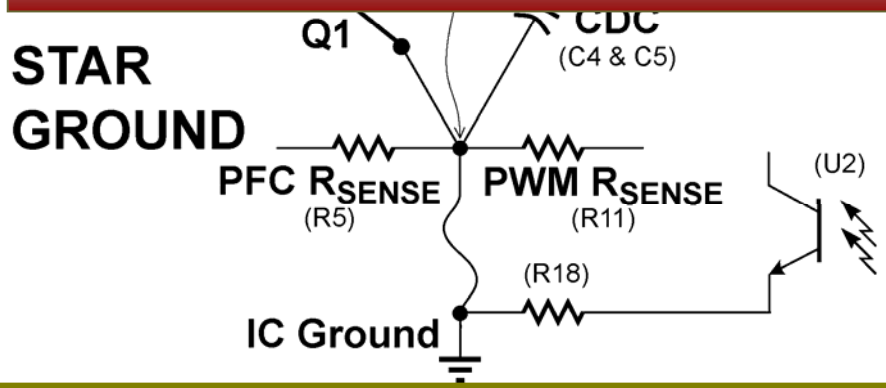
#2: R18 (from the opto islator) must be physically butted against the IC Ground pin.

#3: C4 ... tion.

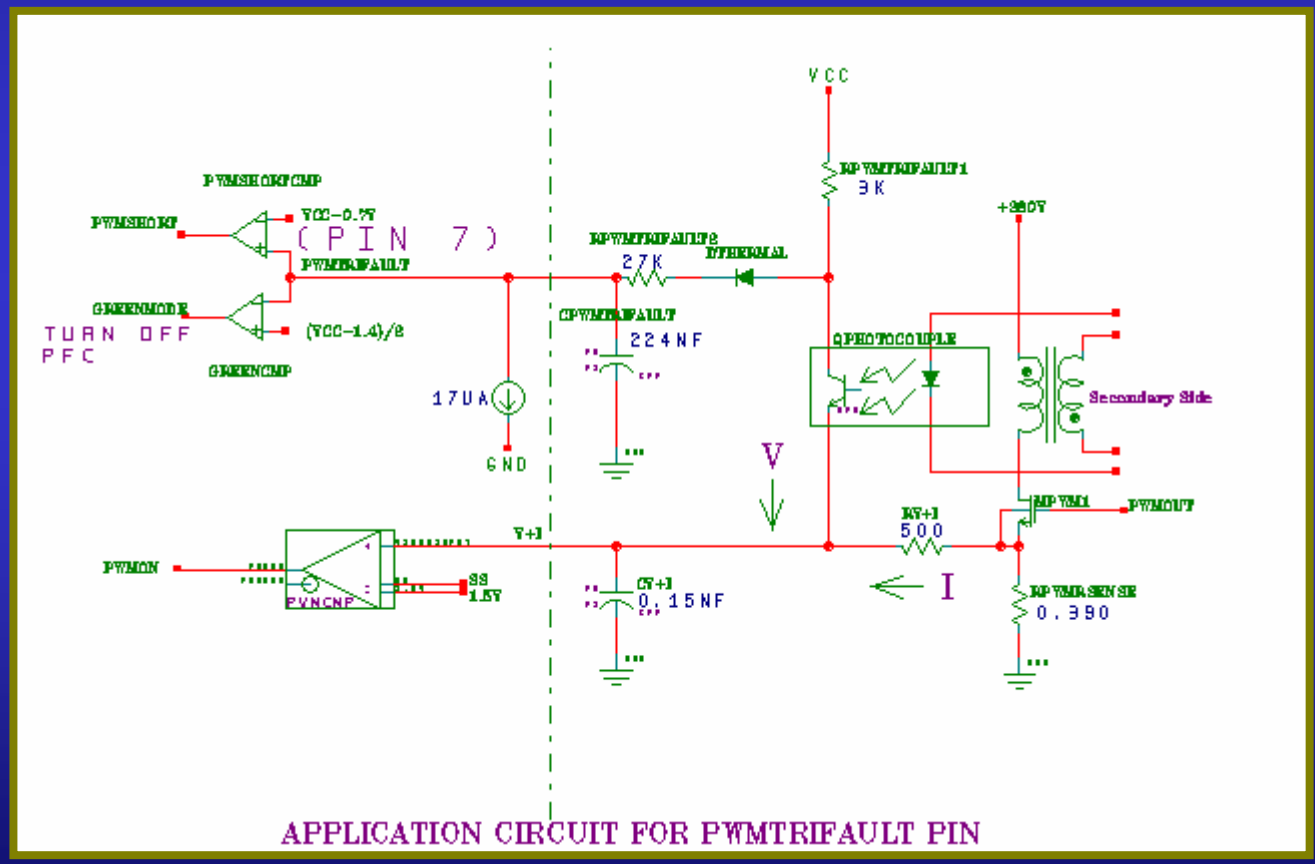
#4: Q1 ... /C5 jun...

Exc... ar" poi...

The entire components Related with V+I (pin 6) have the highest priority

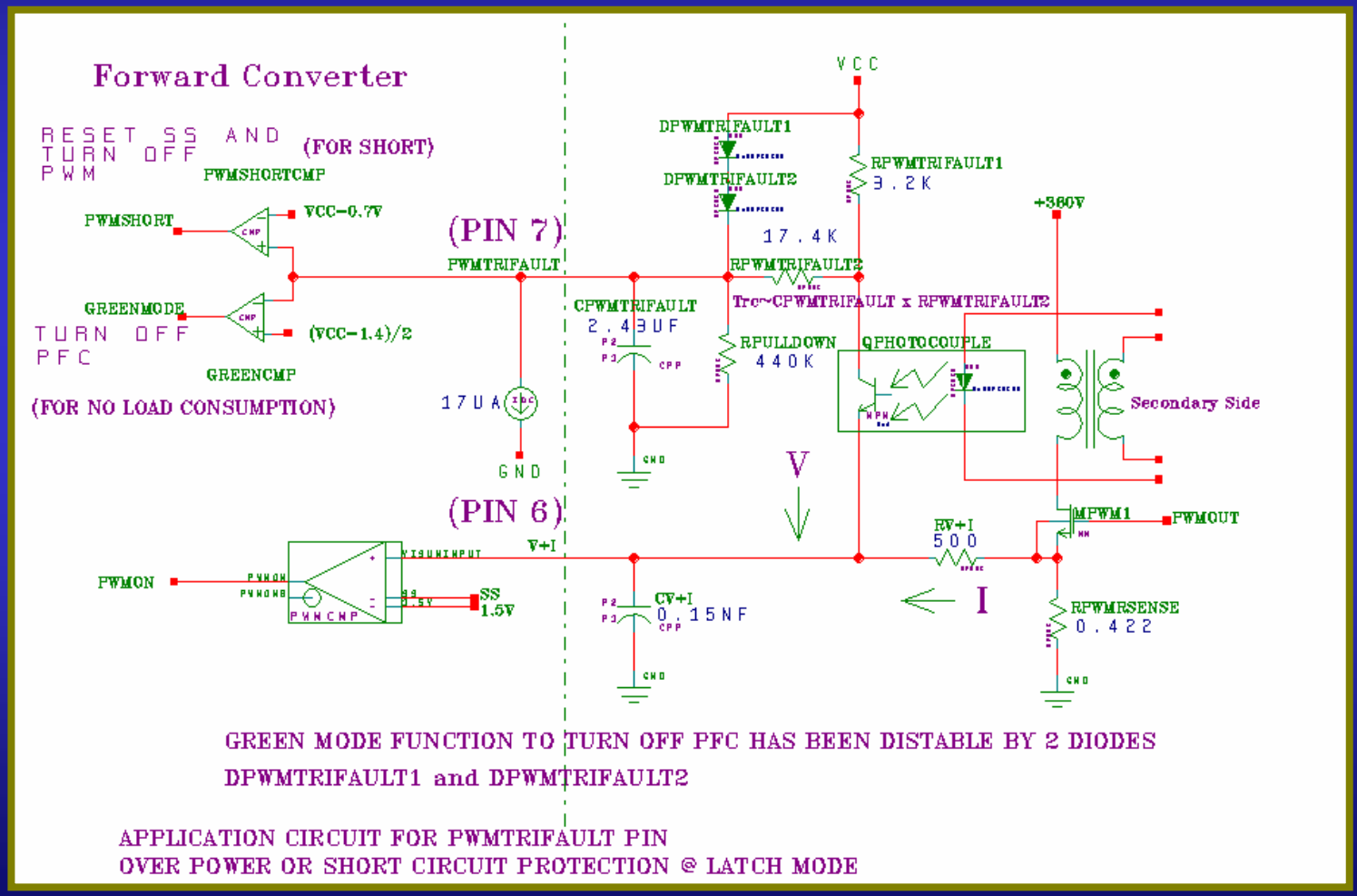


V+I, (pin 6) and PWMtrifault, (pin 7) For FlyBack Converter



APPLICATION CIRCUIT FOR PWMTRIFAULT PIN

V+I, (pin 6) and PWMtrifault, (pin 7) for Forward Converter



CM6807
PFC + Stand By

For 85+
LCD TV or Desk Top