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CM6805A/B

Define Market

- Low Cost PC Power/Clone PC market
- Replace Passive PFC with Active PFC
- Single Range (230Vac only) Power (70% market share)

Topology+controller

Passive to Active PFC using CM6805A/B

- PFC + Single Switch Forward,Dual Switch Forward(base on purchase capability)
- fixed switching frequency (67.5Khz or 100Khz)
  - CM6805A/B: 10 pin SOIC fpfc = fpwm = 67.5Khz(05A) or 100Khz(05B)

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Why chose 6805 series replace passive power supply(cost???)

CM6805 family could drive BOM 20% lower than 6800A

$ 10 pin SOIC PFC/PWM combo allows Less external components (about 14 components less)
$ Leading Edge PFC/Trailing Edge PWM → 450V Bulk Cap can be reduced
$ Digitized PWM maximum duty, 50% → 450V Bulk Cap can be further reduced
$ CM6805 specialized feature with Powder Iron PFC core(230V AC)
$ Single Range Power reduces PFC Mosfet
$ Passive PFC has the higher cost in shipping
• PFC tri-fault and PWM tri-fault →UL1950 (Passive PFC cannot meet it)
• No load consumption spec. cannot be met by Passive PFC; Easy for CM6805 family
• Smooth On/Off which single PFC with single PWM is difficult
$ As results, the BOM cost is lower than Passive PFC

Feature how to reduce power cost

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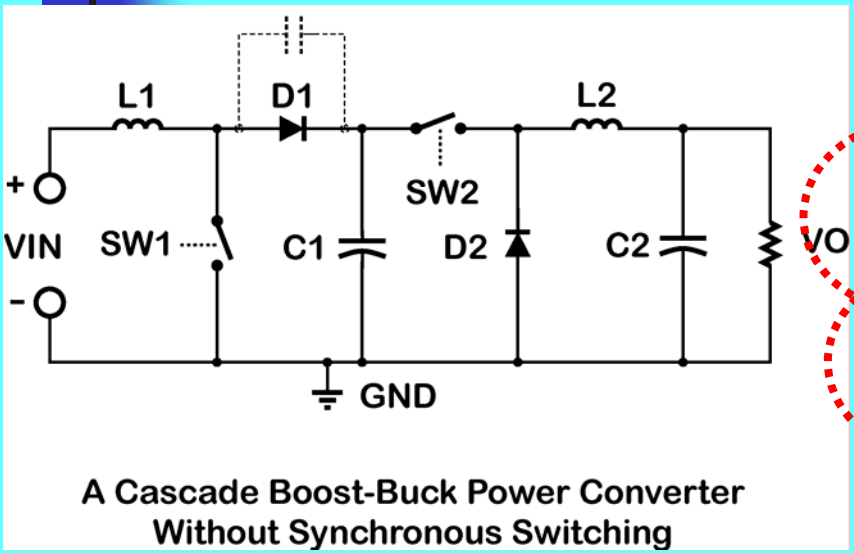
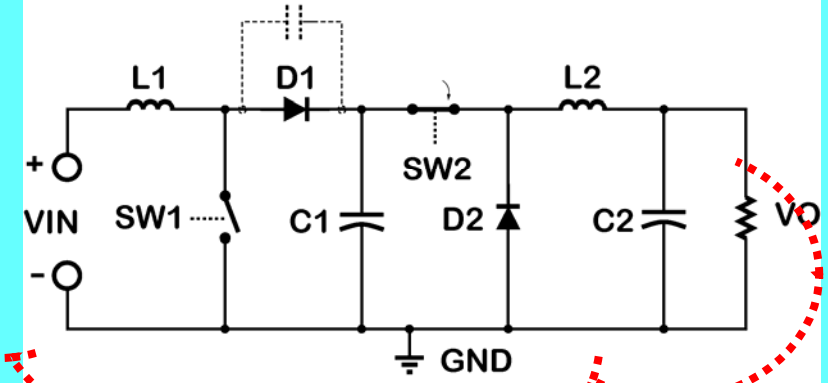
Champion PFC+PWM combo IC benefit

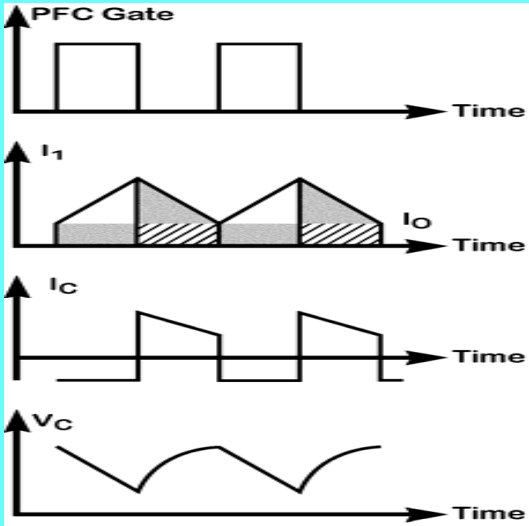


A Cascade Boost-Buck Power Converter Without Synchronous Switching

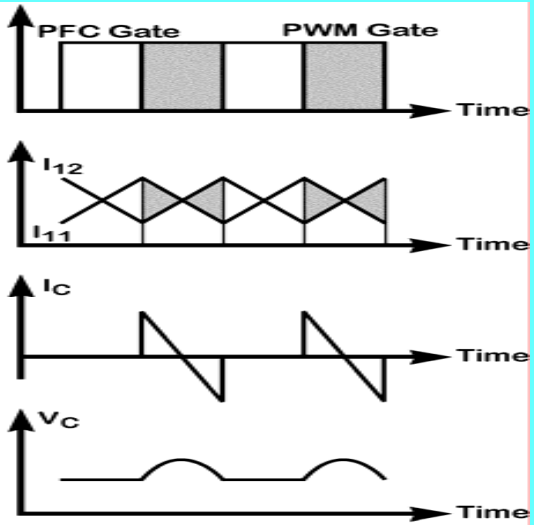
Leading Edge Modulation PFC and Trailing Edge Modulation PWM for PFC Output Ripple Reduction



Synchronous-Switching Cascade Power Converter



Boost Stage with a Constant Current Loss



Cascade Power Stage with Synchronous Switching

- Bulk Cap. up to savings $:0.2

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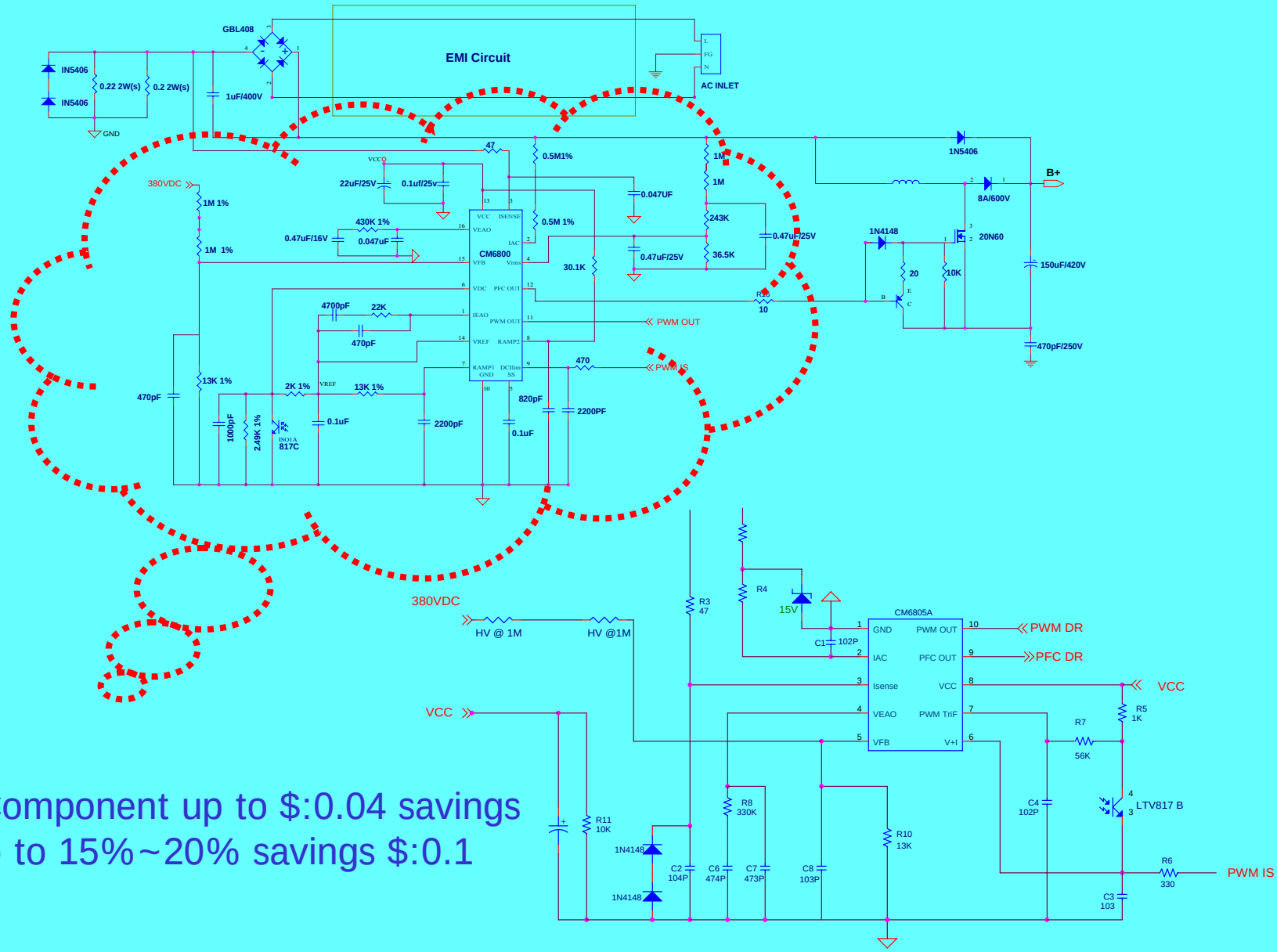
- CM6800 VS CM6805A/B part count



- External Component up to $:0.04 savings
- Ic Cost up to 15%~20% savings $:0.1

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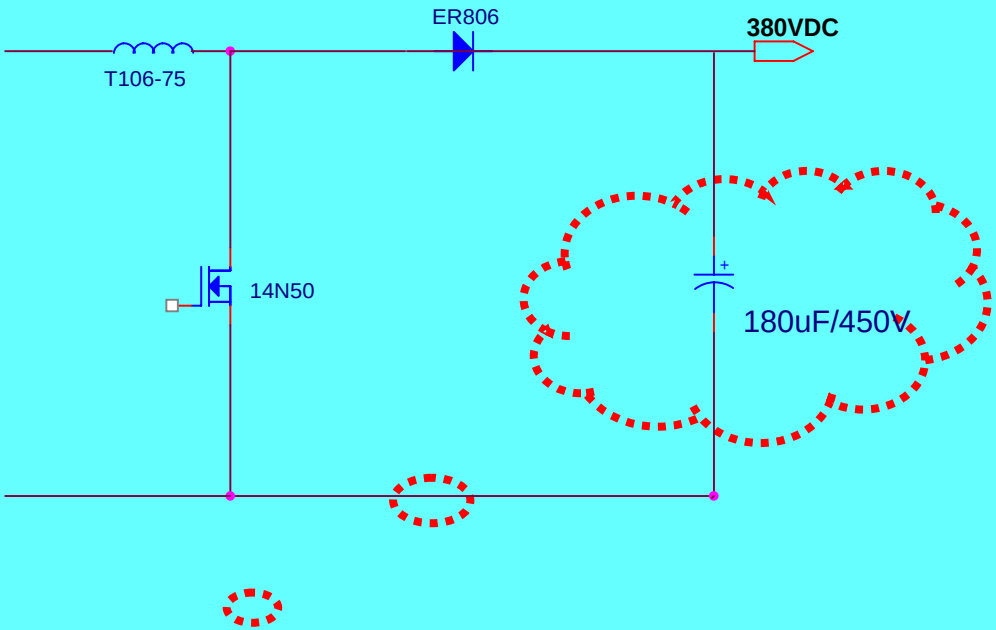
Digitized PWM maximum duty, 50%
→450V Bulk Cap can be further reduced



V tolerance +-20%~tolerance (0)
M tolerance –10%~+20%(x)
V tolerance (V) Bulk cap up to $:0.05(7%) savings

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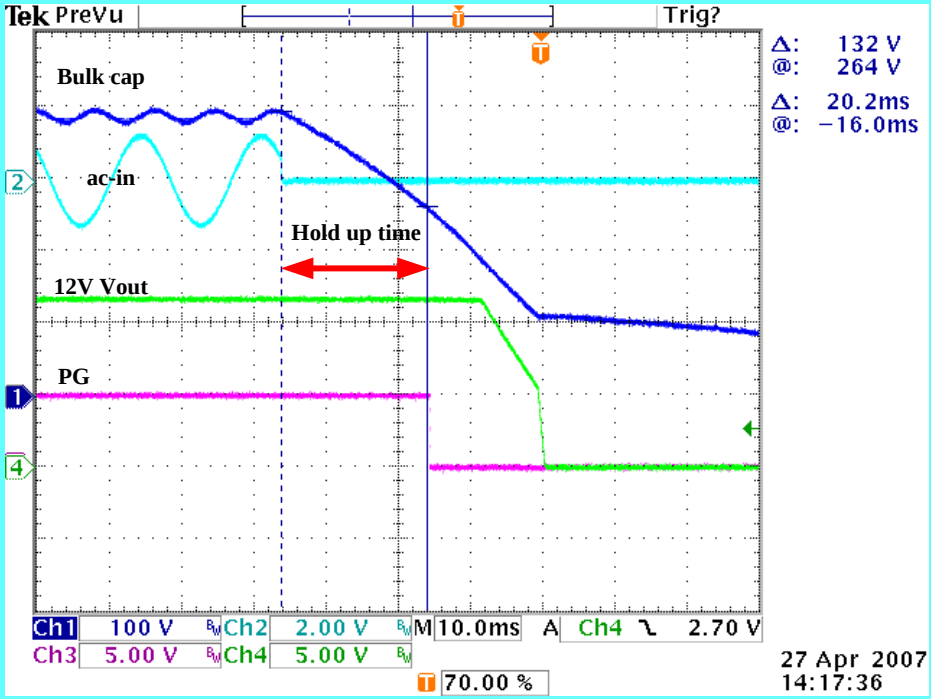

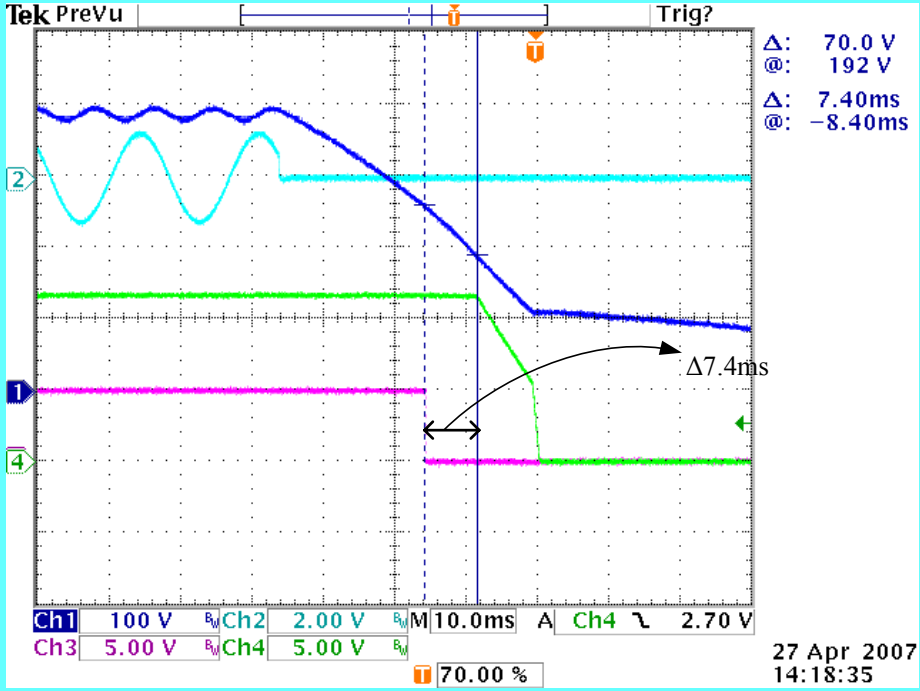

Hold up time can gain 6ms least, still keep PG to main output >1ms lead(1.4ms).

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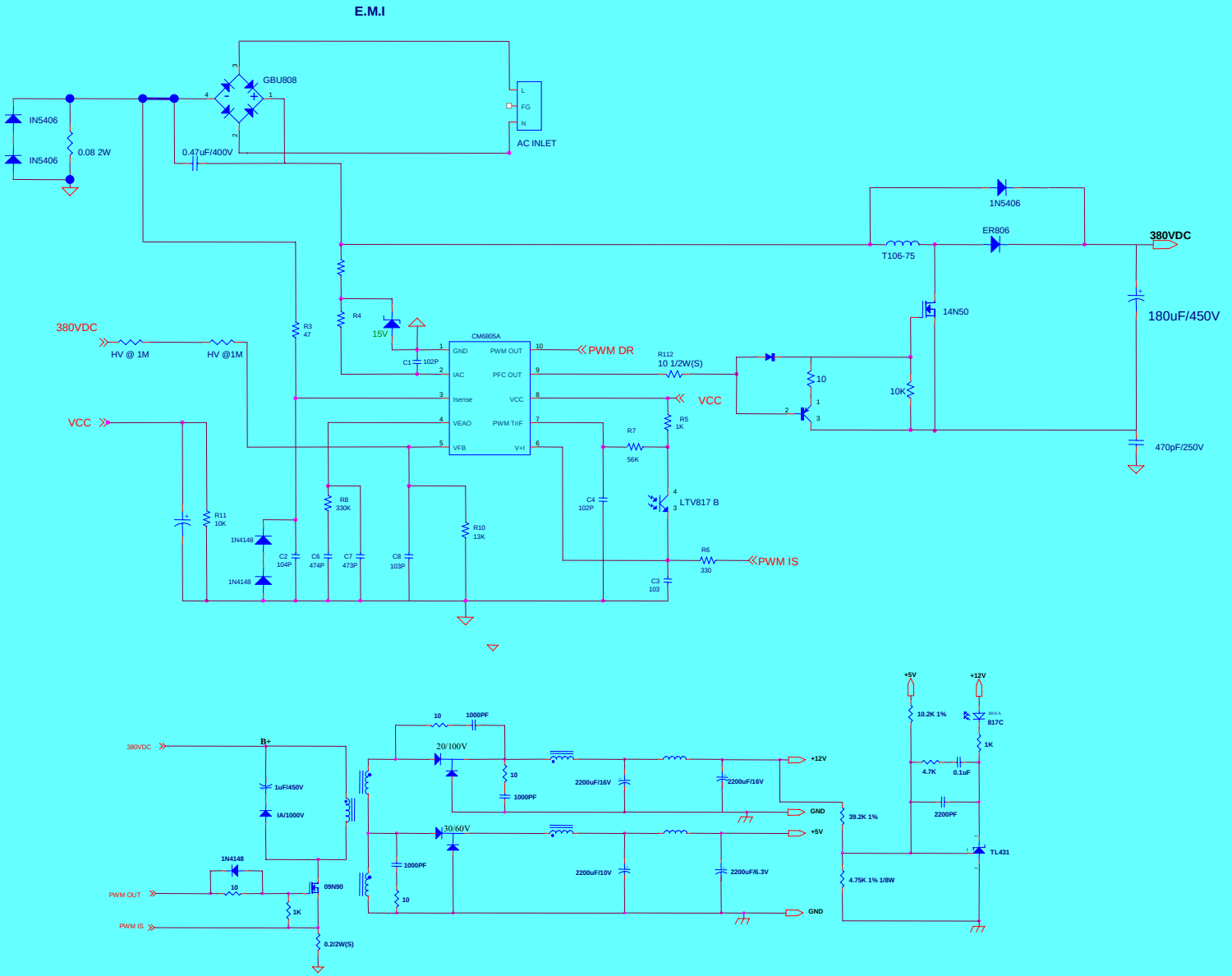
Application circuit



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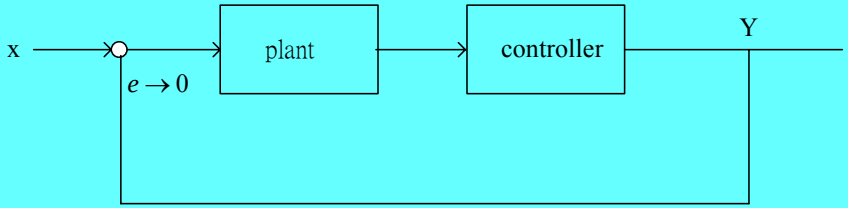
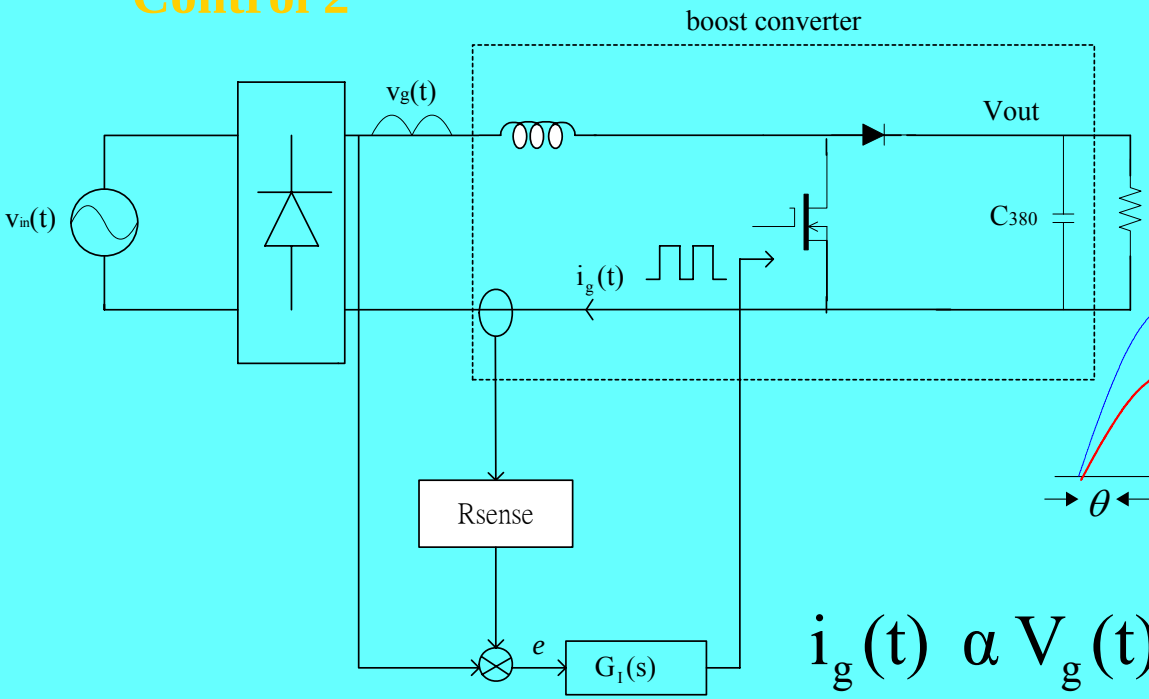
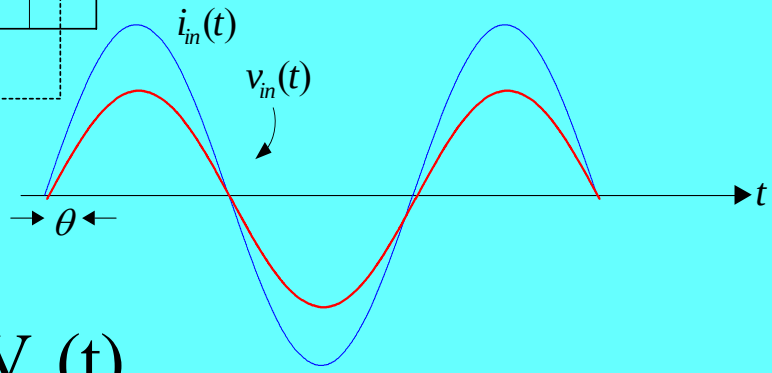
Goal:P.F&V380

Control 1



Control 2





$$i_g(t) \ \alpha \ V_g(t)$$

V380????

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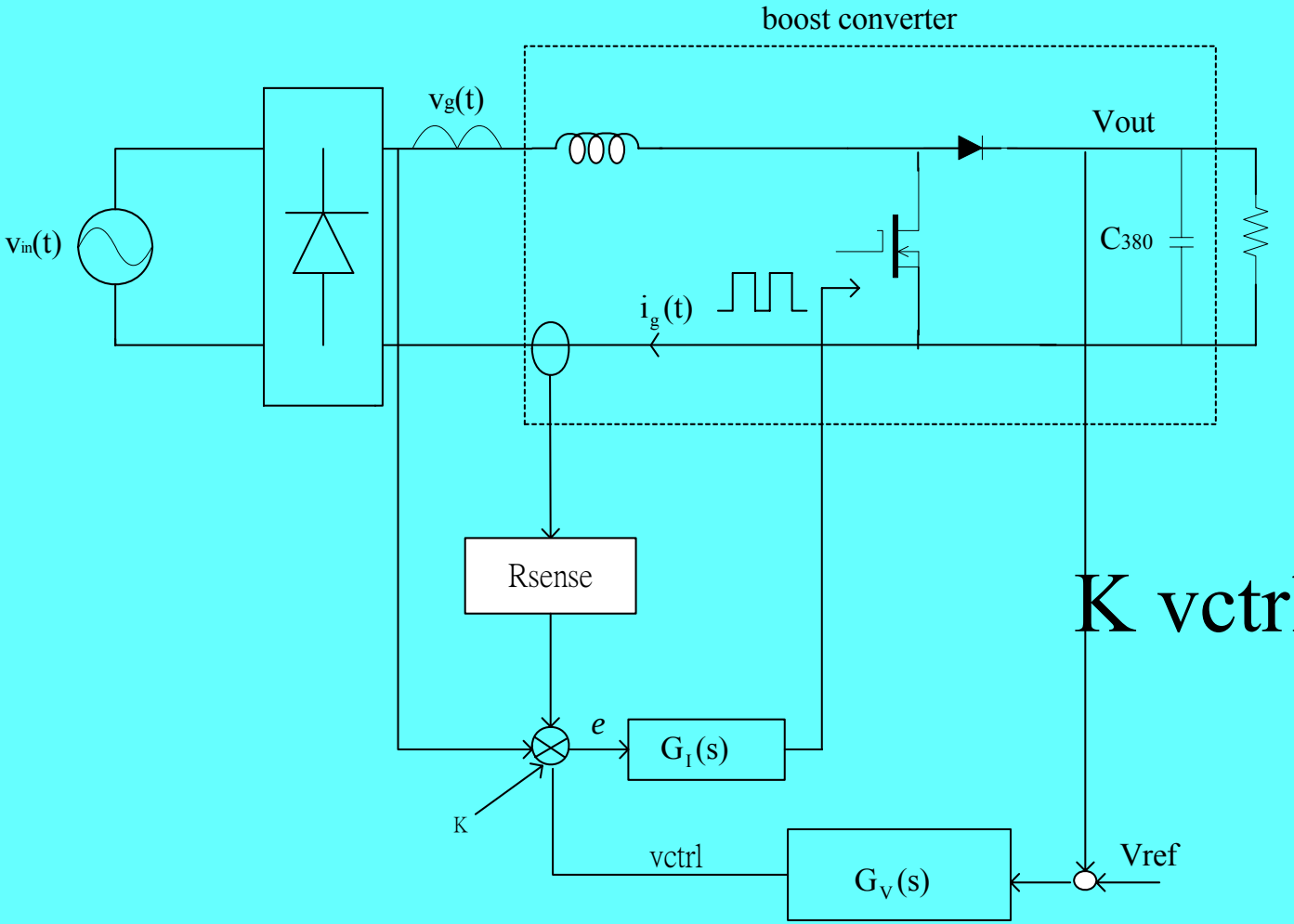
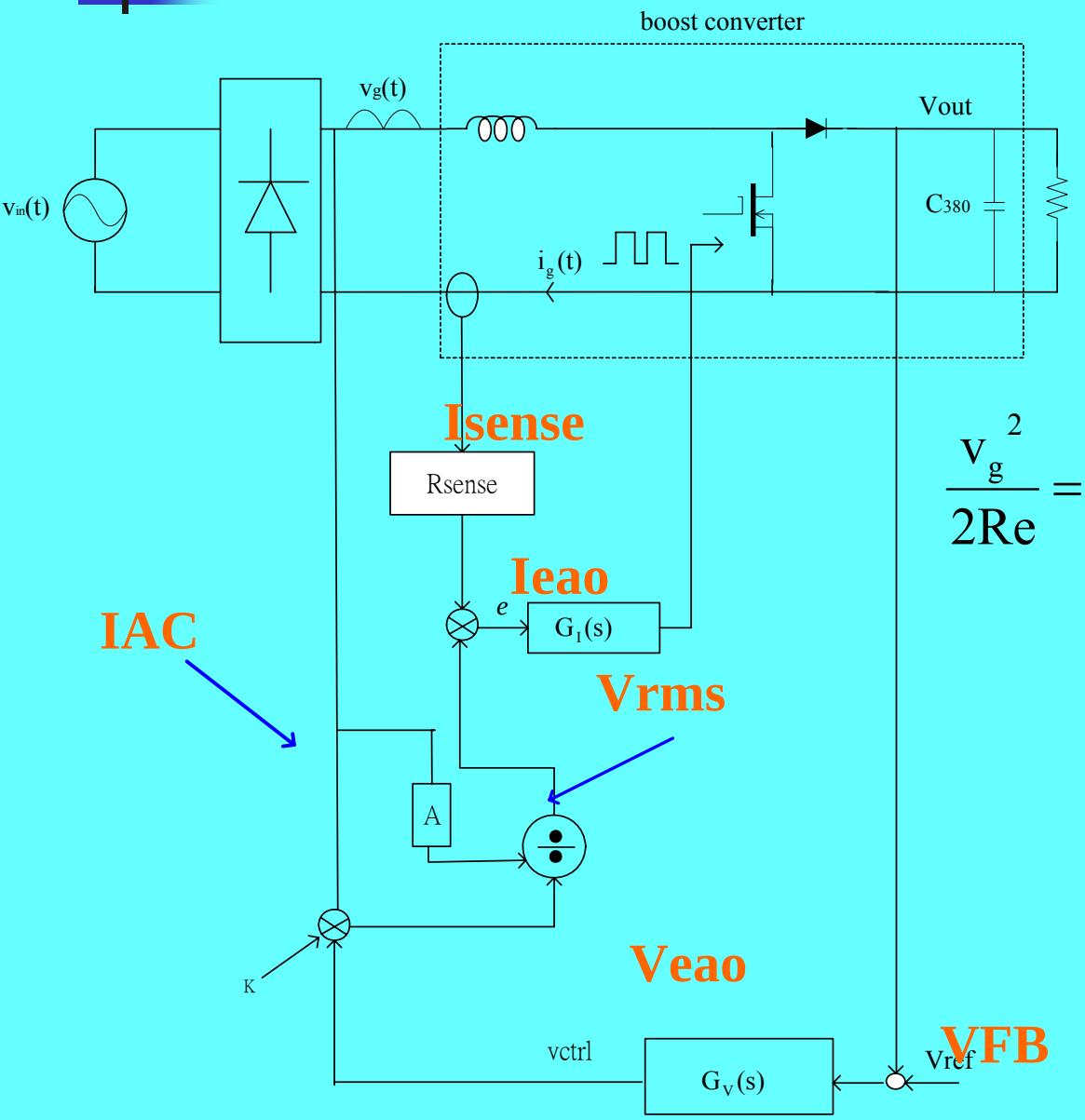
PFC&regulation



$$K\ vctrl\ v_g(t)\ \alpha\ i_g(t)$$

PFC&regulation



$$\frac{v_g^2}{2Re} = \frac{V_{380}^2}{R_L} \xrightarrow{A} \frac{v_g^2}{2ARe} = \frac{V_{380}^2}{R_L}$$

$$A = v_g^2$$

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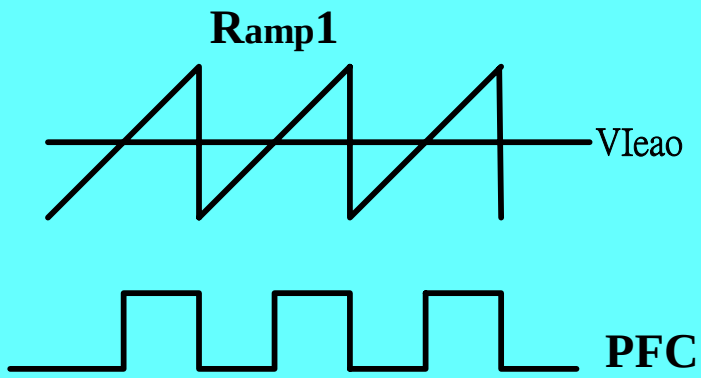
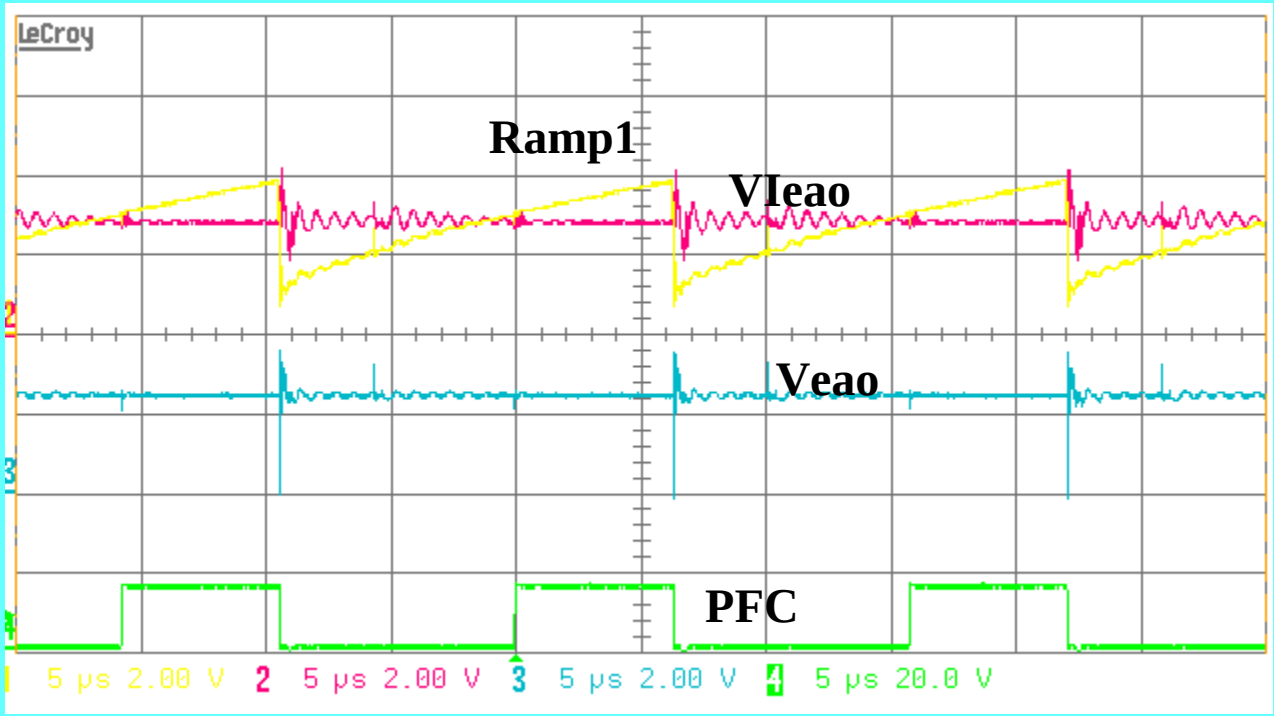
Waveform discuss

PFC(Leading-edge)





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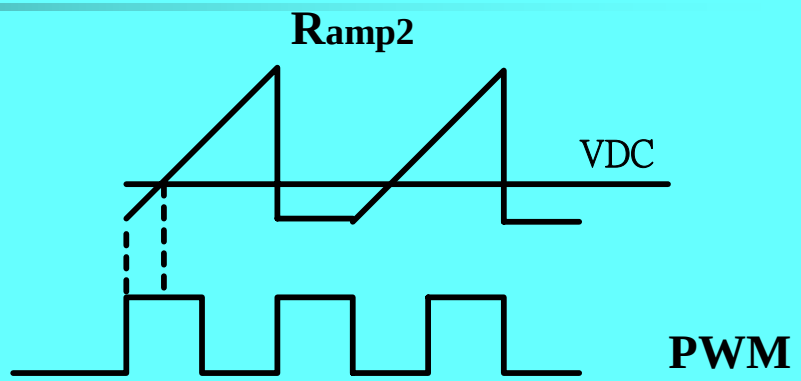
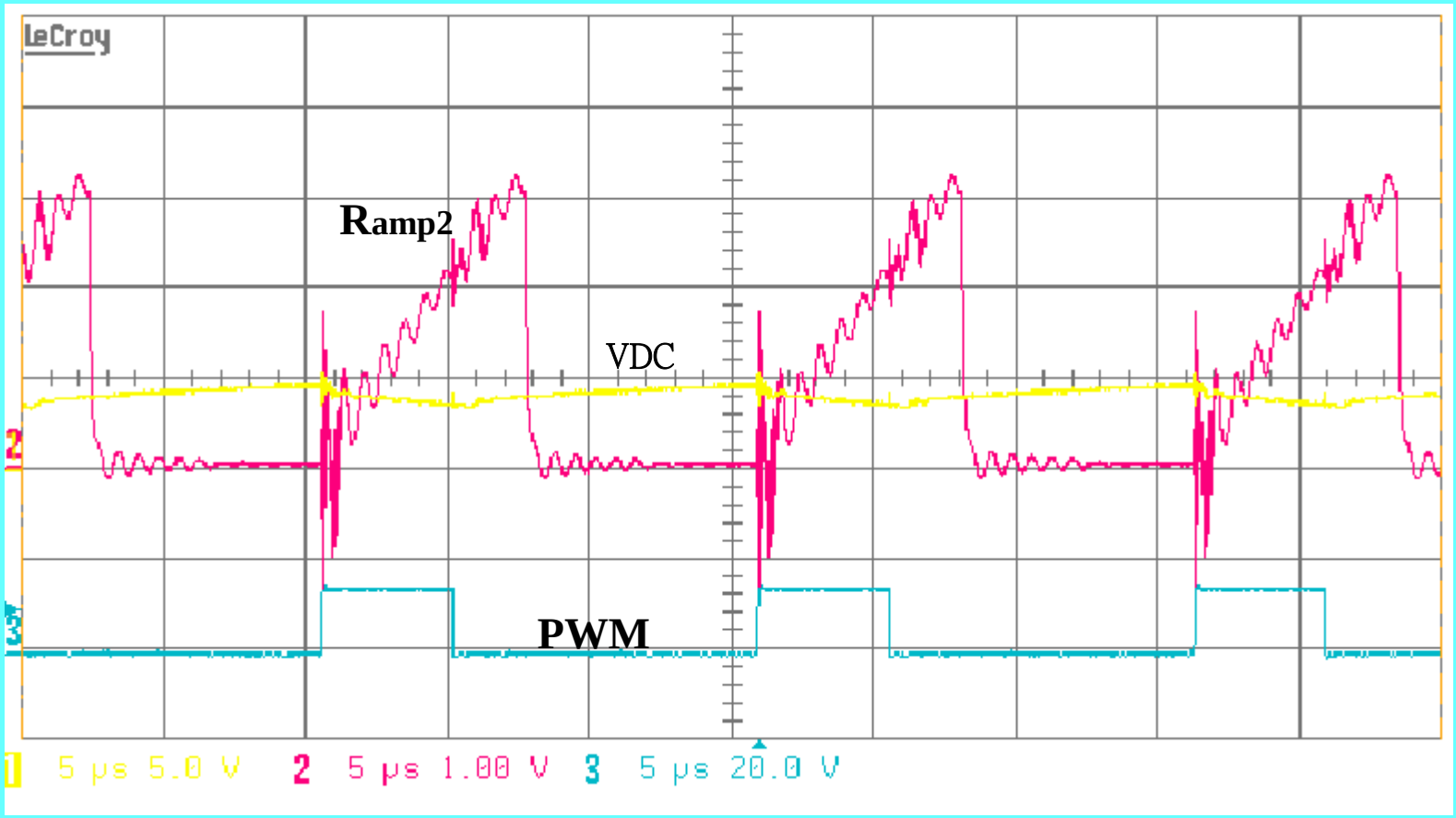
Waveform discuss

PWM(trailing-edge)





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CM6805A/B/CM6903 PFC Controller:

Leading Edge Modulation
with Input Current
Shaping Technique

(I.C.S.T)

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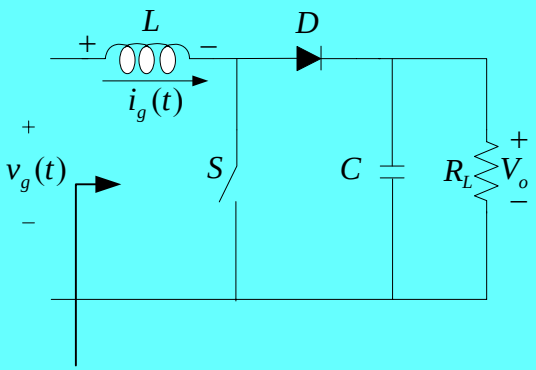
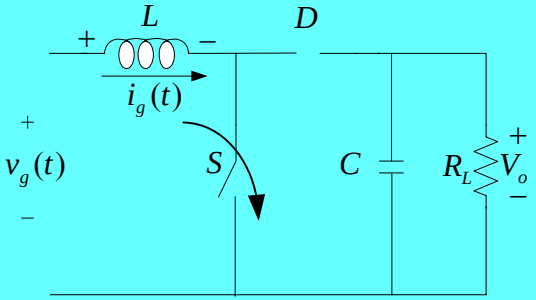
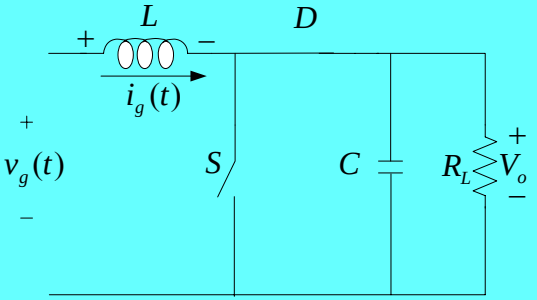
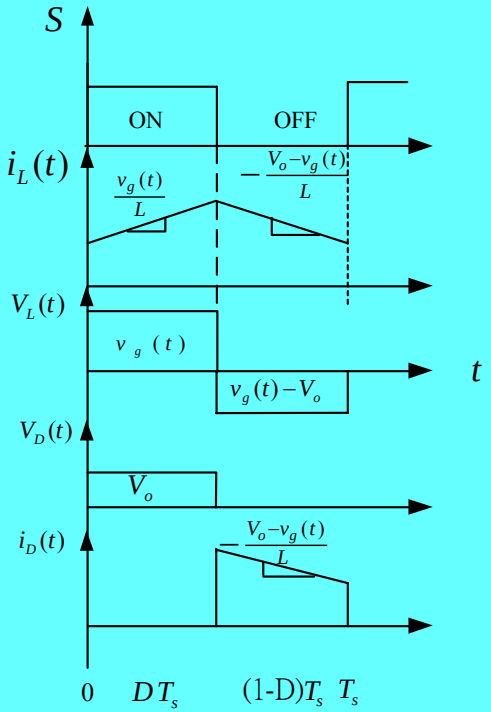
Boost-converter



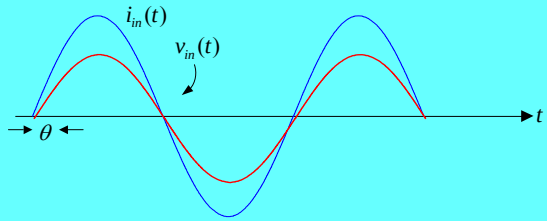




Re



$$R_e = v_g / i_g$$



$$< i_g > = < i_L >$$

$$v_g \times < i_L > \approx V_{out} \times < i_d >$$

$$< i_d > = (1-d)^2 \times V_{out} / R_e$$

$$V_{out} / V_g = 1/(1-d)$$

$$< i_d > = \frac{V_{out}}{R_e} \times \frac{t_{off}}{T_{sw}}$$

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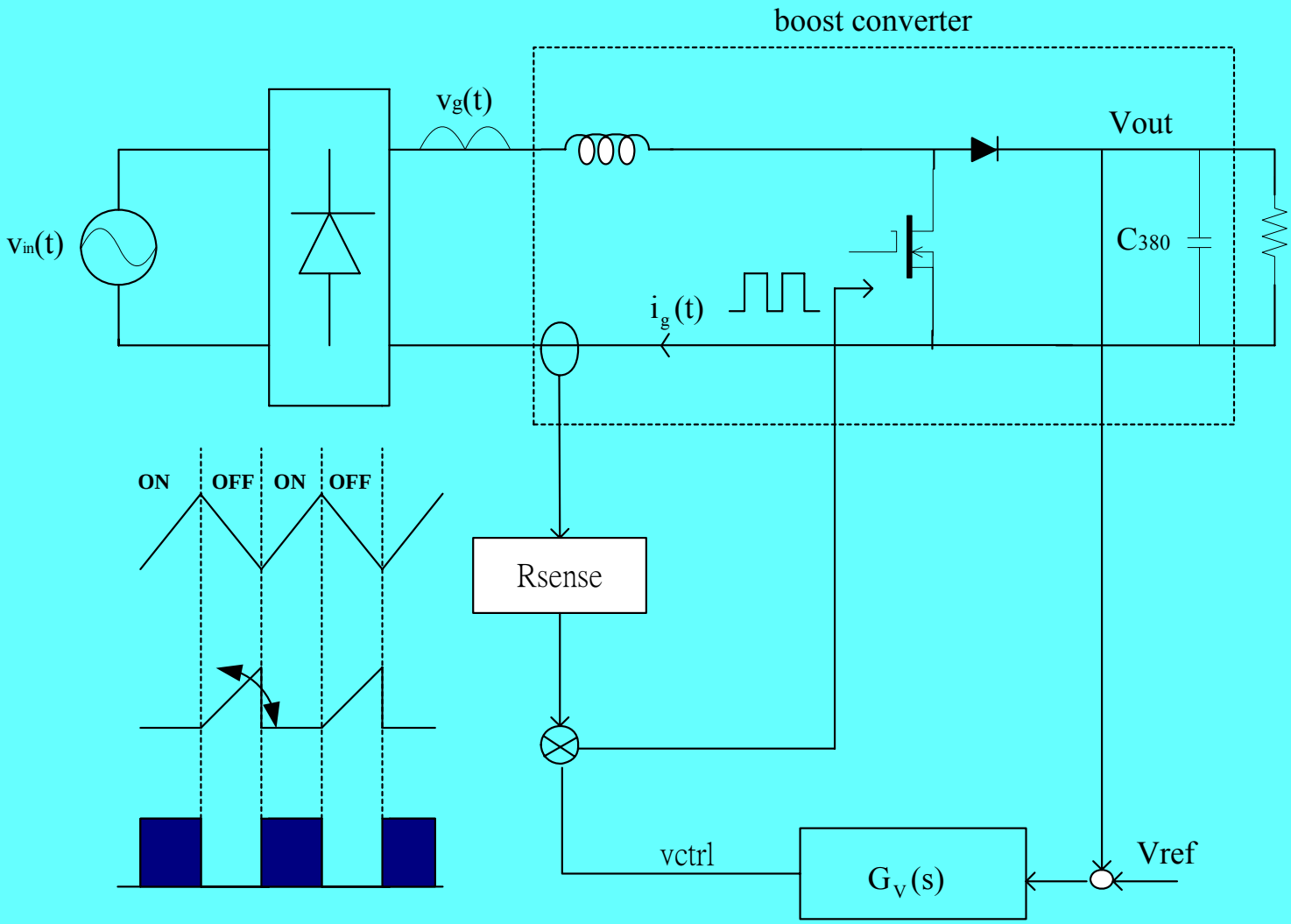
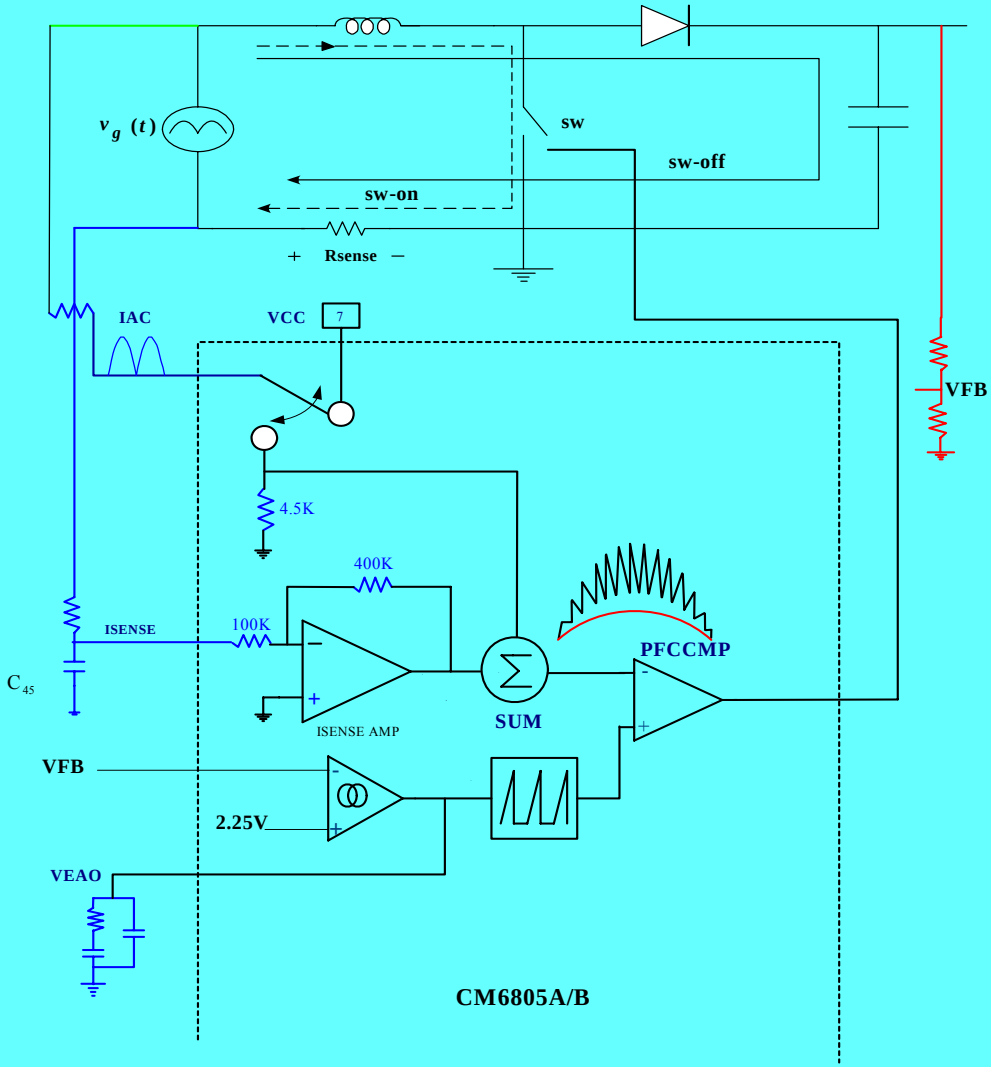

boost converter
vg(t)
Vout
vin(t)
C380
ig(t)
ON
OFF
ON
OFF
Rsense
vctrl
Gv(s)
Vref


v_g (t)
sw
sw-off
sw-on
+ Rsense −
IAC
VCC
7
VFB
4.5K
400K
ISENSE
100K
C_{45}
ISENSE AMP
SUM
PFCCMP
VFB
2.25V
VEAO
CM6805A/B

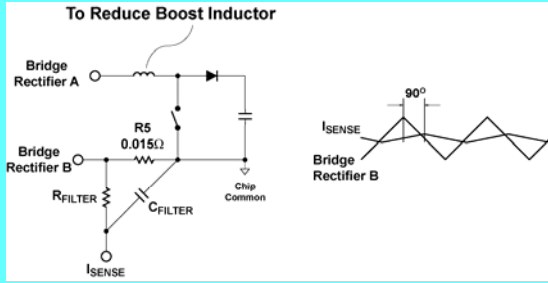
Rac filter(Pin2)

- Rac 作為slope compensation斜率補償用
- 調整作為THD enhance
- Rac以IC內部阻值作為選擇依據

Iac impedance	Rac	Part.No.
40k	4~6M	CM6805A

Isense(Pin3) compensation(CM6800同)

- Isense 之訊號需filter 為 1/6~1/10 switching frequency



$$\text{Isense}_{\text{frequency}} = \frac{1}{2\pi \times R_{is} \times C_{is}} = \frac{1}{6} \sim \frac{1}{10} f_s$$

R_{is}選用47Ω

$$= \frac{1}{2\pi \times 47 \times C_{is}} = \frac{1}{6} \sim \frac{1}{10} f_s = 6750$$

$$C_{is} = 301.1n \sim 50.9nF \qquad \text{可選用} 0.1\mu F$$

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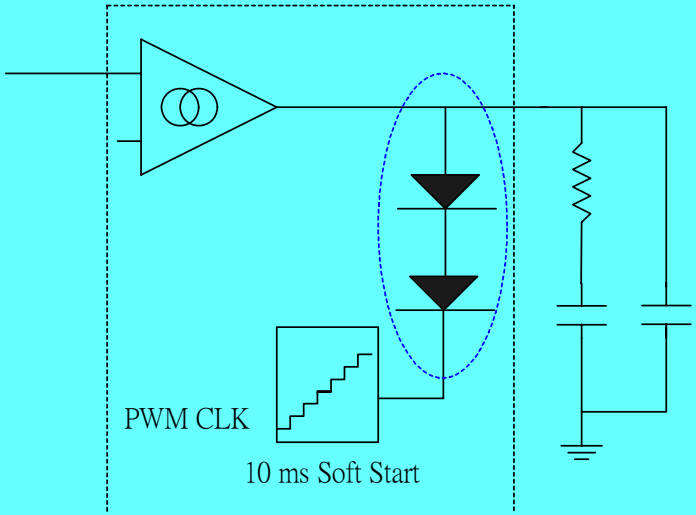
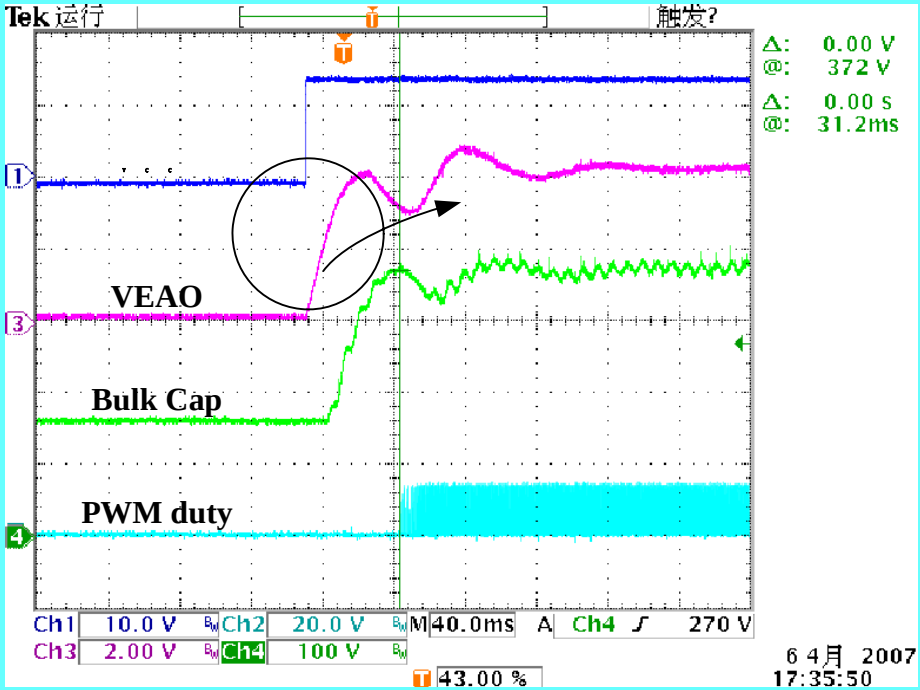
PFC Soft Star

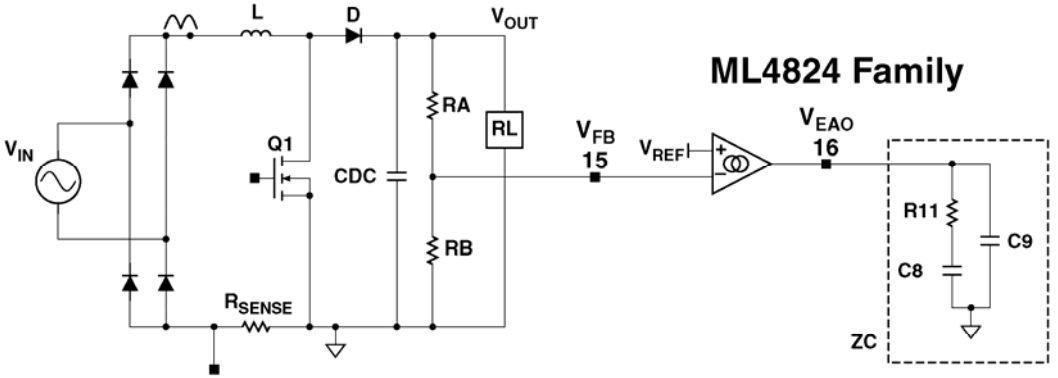


CM6805A/B



Veao(pin4) compensation(CM6800同)

- VEAO的補償為乘上zero-pole network， 一般選擇其unity-gain(crossover-frequency)為0.5 line-frequency=25Hz or 30Hz，zero的位置為0.1pole。



$$\because \frac{\Delta V_{OUT}}{\Delta V_{EAO}} = \frac{P_{IN\ AVERAGE}}{V_{OUT} \times \Delta V_{EAO} \times S \times C_{DC}} \quad (1)$$

$$\because \frac{\Delta V_{FB}}{\Delta V_{OUT}} = \frac{R_B}{R_A + R_B} = \frac{2.5V}{380V} \quad (2)$$

$$\because \frac{\Delta V_{EAO}}{\Delta V_{FB}} = Gm \times Z_C \quad (3)$$

$$\therefore \text{Loop Gain} = \frac{\Delta V_{OUT}}{\Delta V_{EAO}} \times \frac{\Delta V_{FB}}{\Delta V_{OUT}} \times \frac{\Delta V_{EAO}}{\Delta V_{FB}} = \frac{P_{IN\ AVERAGE} \times 2.5V}{V_{OUT} \times \Delta V_{EAO} \times S \times C_{DC} \times 380V} \times Gm \times Z_C \quad (4)$$

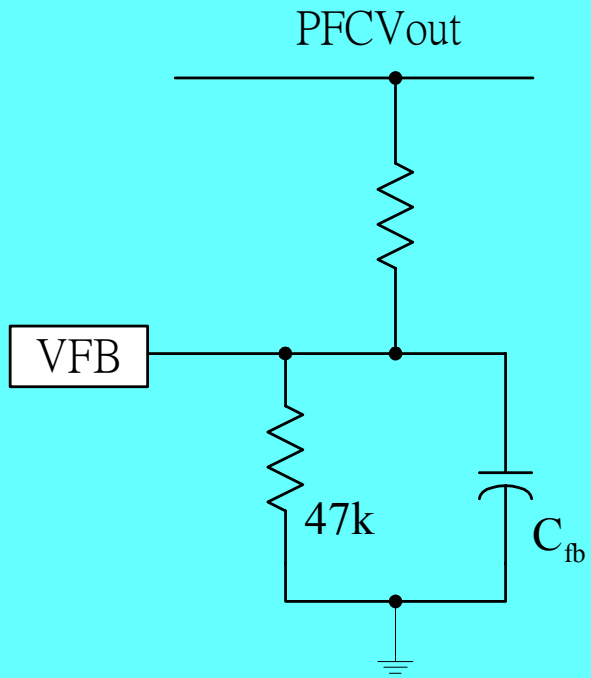
VFB Pin(5)

$$\frac{1}{2\pi \times R_{fb} \times C_{fb}} > 150Hz$$

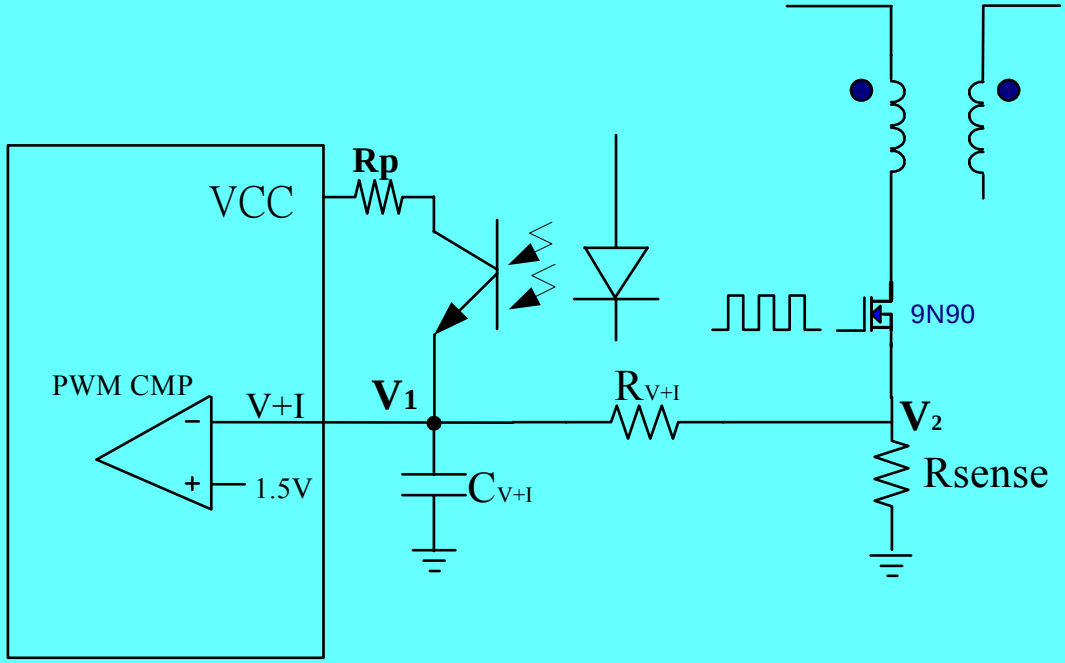
$$Ex: \frac{1}{2\pi \times 47k \times C_{fb}} > 150Hz$$

$$C_{fb} < 22nF$$

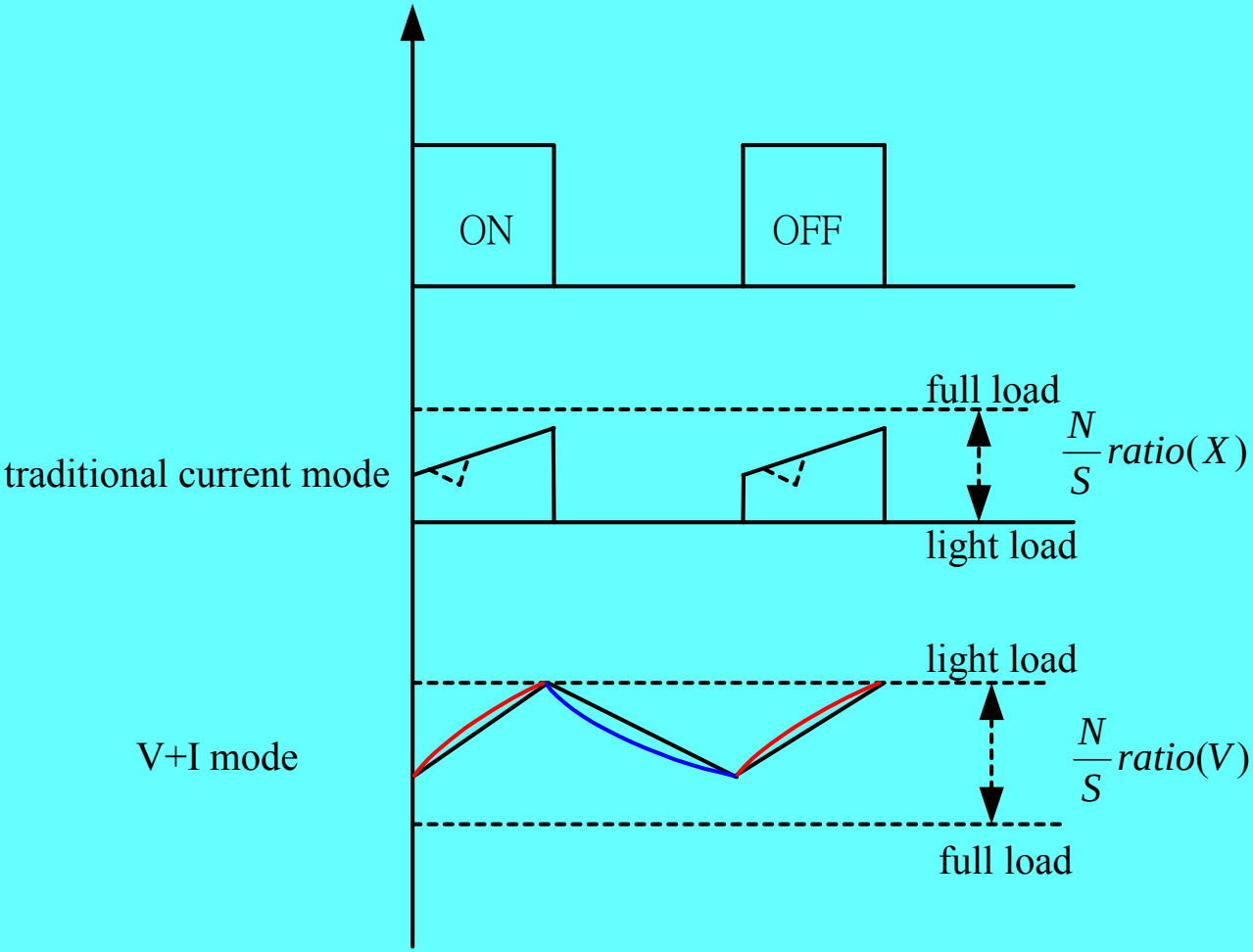
C_{fb}可選用102或103



PWM Stage



$$Rp = \frac{VCC - V_{CE} - (V + I)}{\text{photo couple curret}} = \frac{15 - 1 - 1.5}{10mA} = 1.25K$$


ON
OFF
full load
traditional current mode
$\frac{N}{S} ratio(X)$
light load
light load
V+I mode
$\frac{N}{S} ratio(V)$
full load

$$R_{V+I} = \frac{V_{1.5(V+I)} - V_{RsensePeak}}{\text{photo Couple Current(Full Load)}}$$

$$= \frac{1.5 - V_{RsensePeak}}{\text{Photo Couple Current(Full Load)}}$$

一般約取$V_{RsensePeak}$爲1.25V

$$= \frac{0.25}{\text{Photo Couple Current(Full Load)}0.5\text{mA}}$$

協助提升系統的暫態響應能力，一般而言，
設計目標是讓控制迴路和45度相位邊限 (phase margin) ，
C_{V+I}與Rsense極點控制濾波在開關頻率內。

$$C_{V+I} = \frac{1}{2\pi\ R_{V+I}\ fsw} = \frac{1}{2\pi\ 500\ 67K} \approx 4700PF$$

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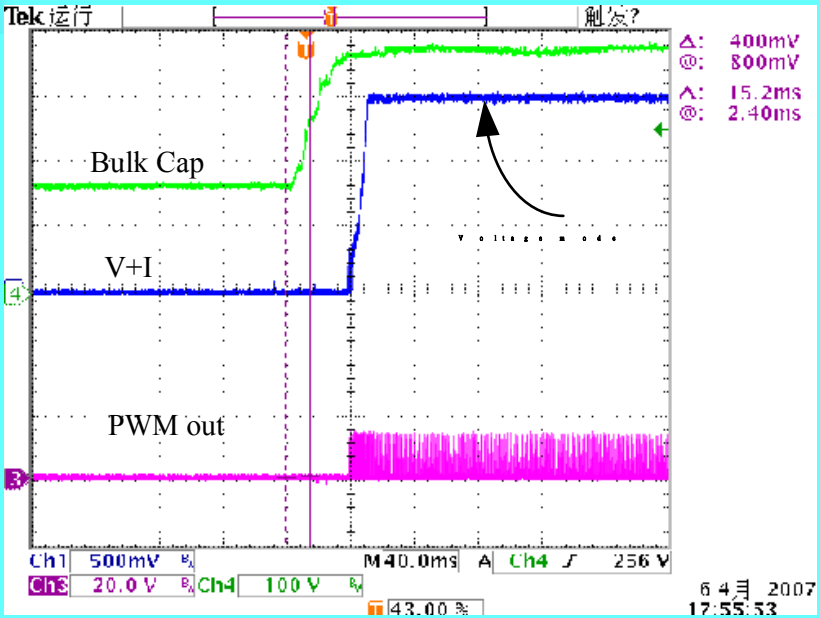
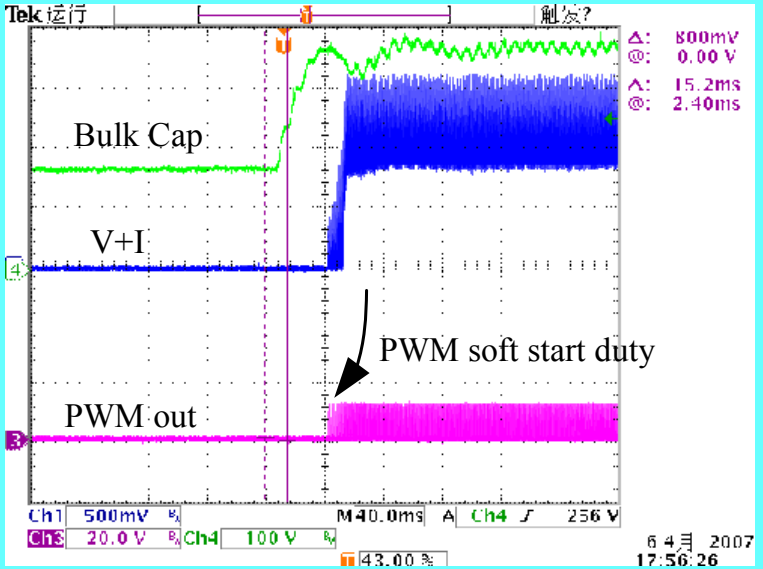
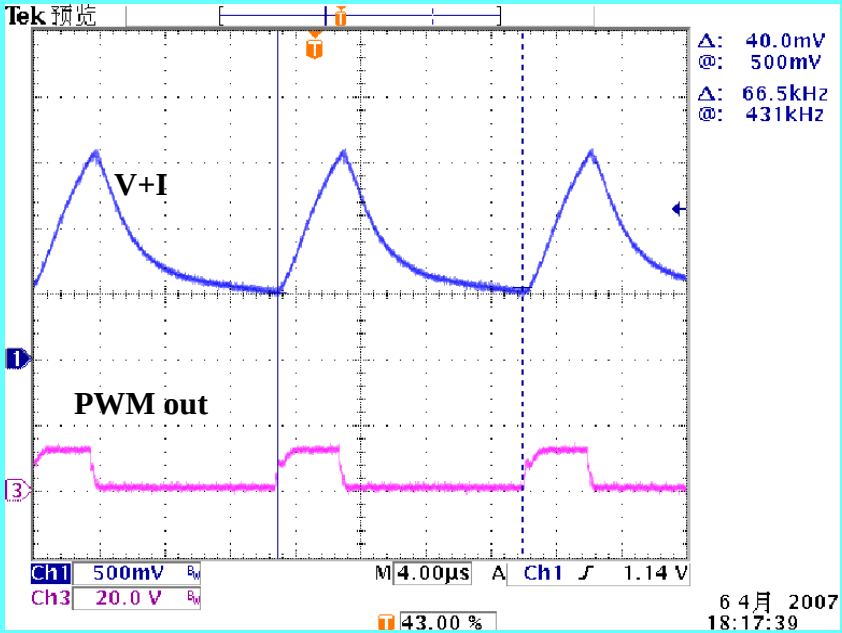
V+I (Pin6)







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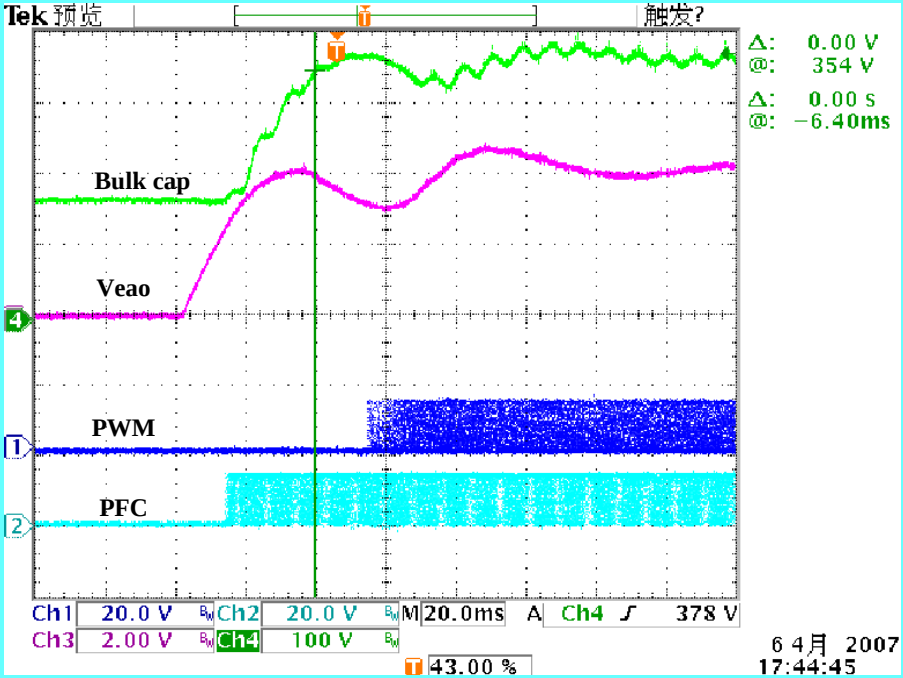
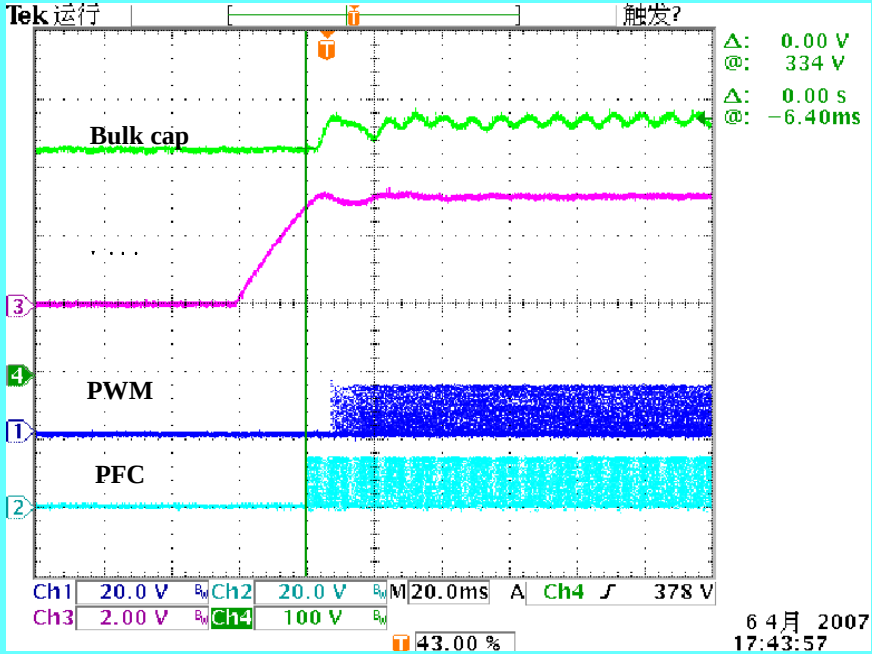
PFC PWM timing





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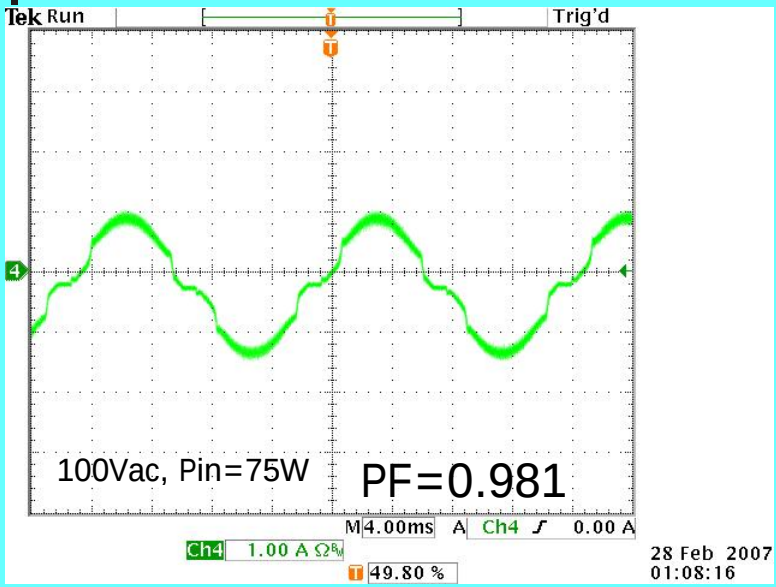
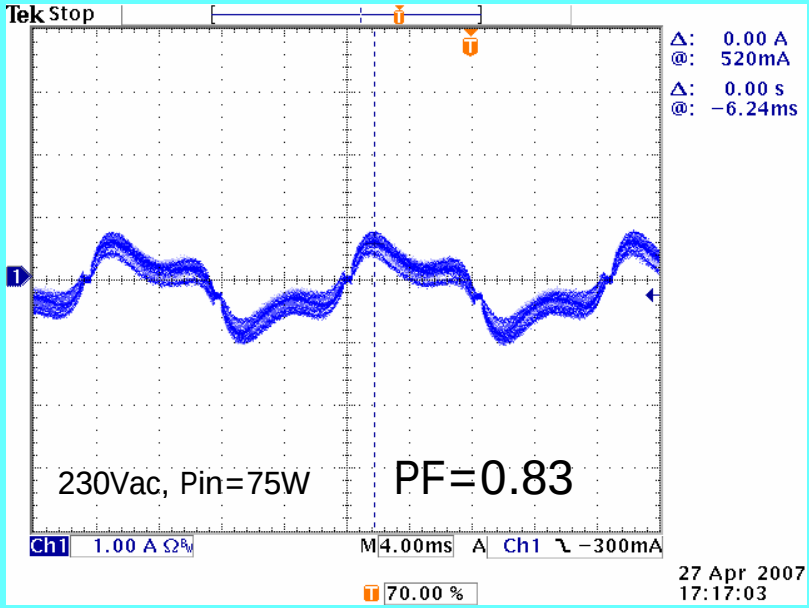
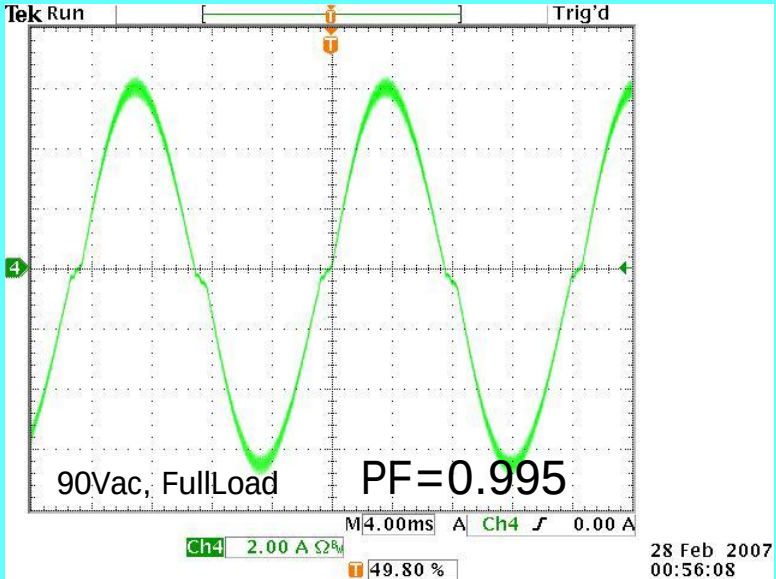
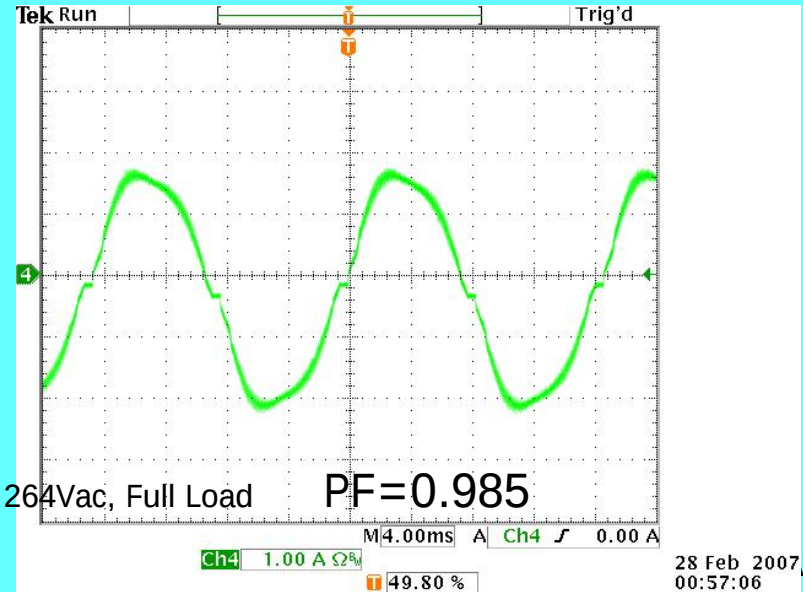
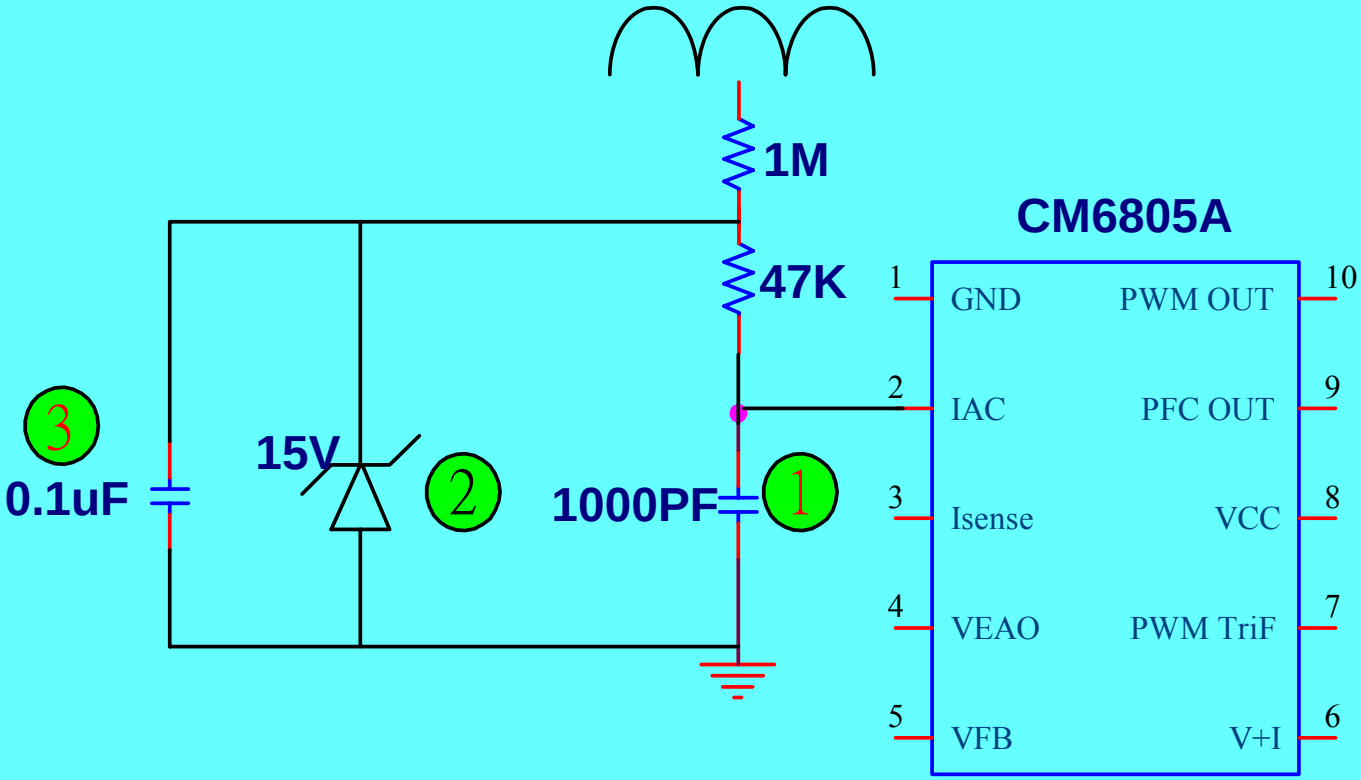








Improve and Enhance THD



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Disable PWM skipping