Industrial Trend

Single Switch Forward → Dual Switch Forward

CM6802A/B

Dynamic Soft PFC

+

Dual Switch Forward

like a ZVS without any extra ZVS circuit

for

EPA/80++ Power

黃新年

Jeffrey H. Hwang

80++
CM6802A/B

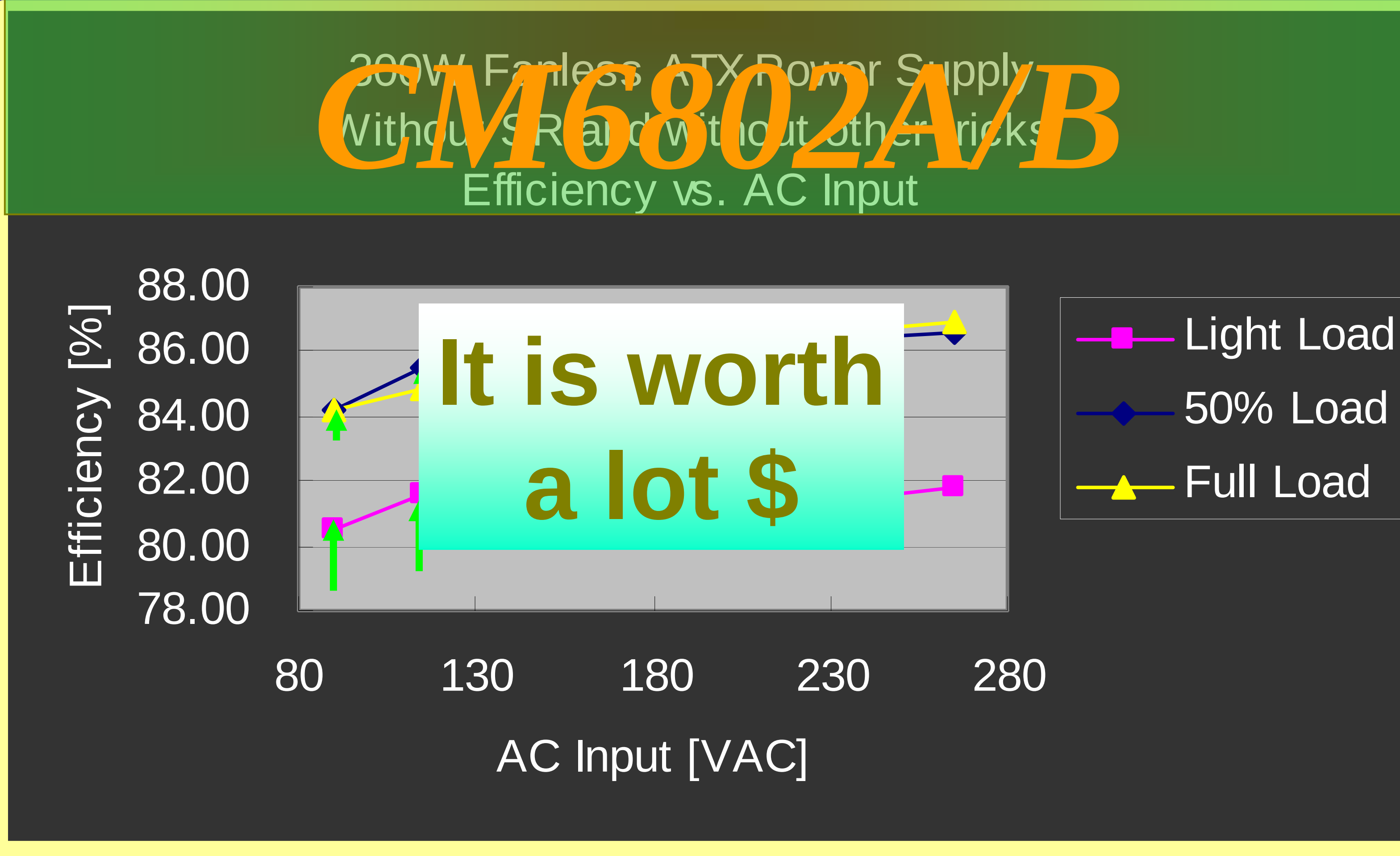
Efficiency goes up

1.5% to 2% higher!

(CM6802A/B vs. CM6800A)

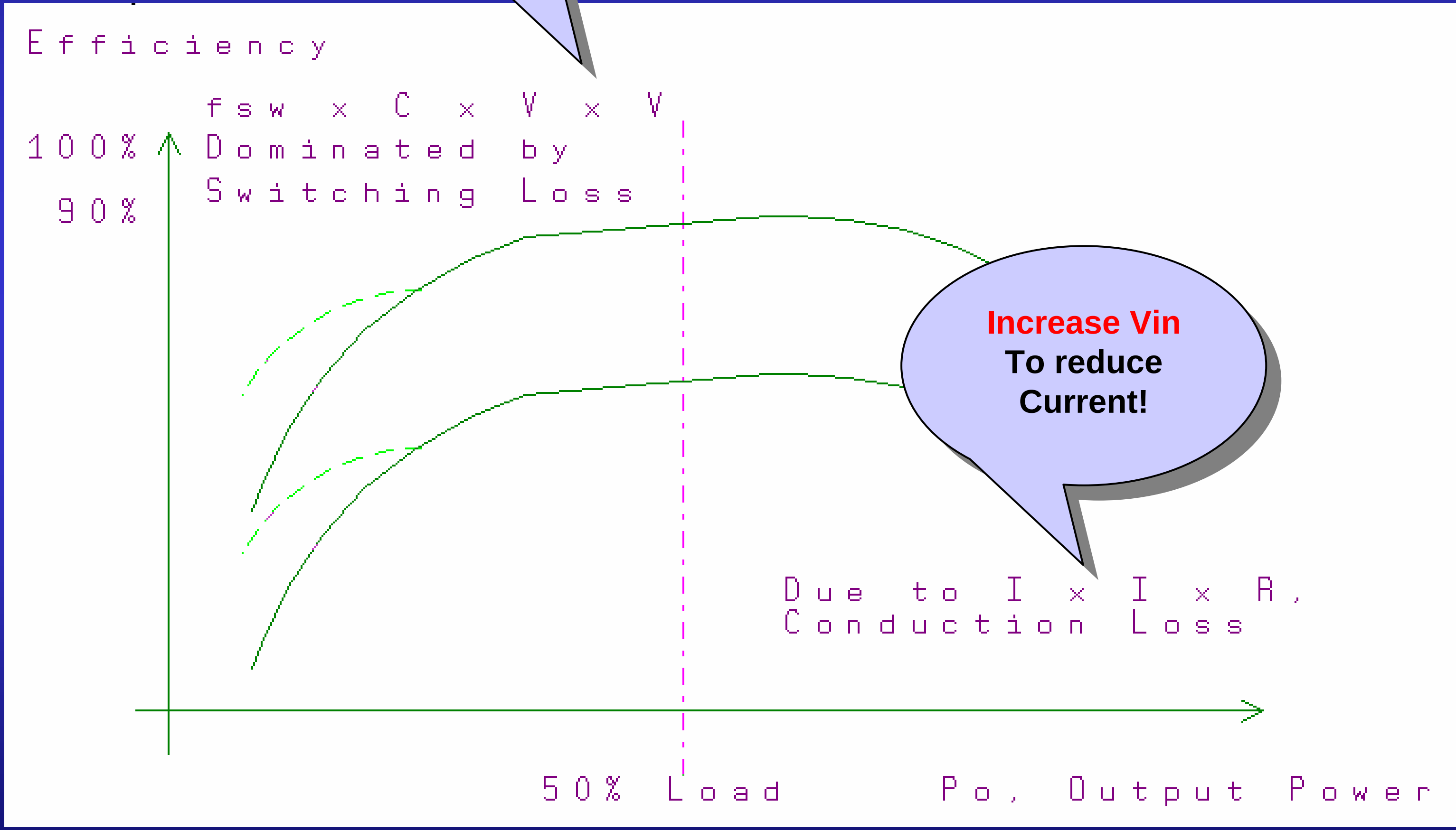
80++

CM6802A/B


300W Fanless ATX Power Supply
Without SR and without other tricks
Efficiency vs. AC Input
Efficiency [%]
88.00
86.00
84.00
82.00
80.00
78.00
80
130
180
230
280
AC Input [VAC]
Light Load
50% Load
Full Load
It is worth
a lot $

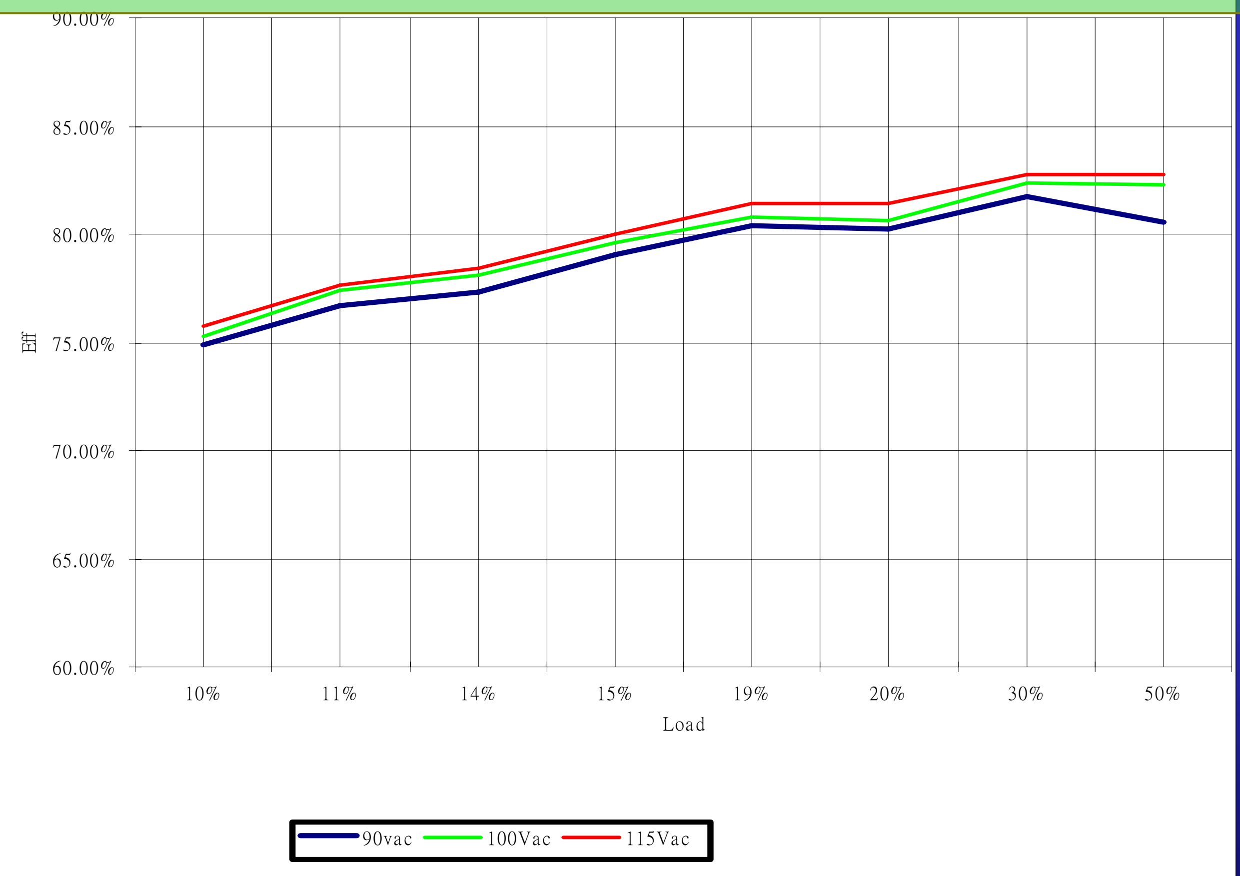
Usually, ...roportional to cost

Reduce Vin
To reduce Switching Loss!

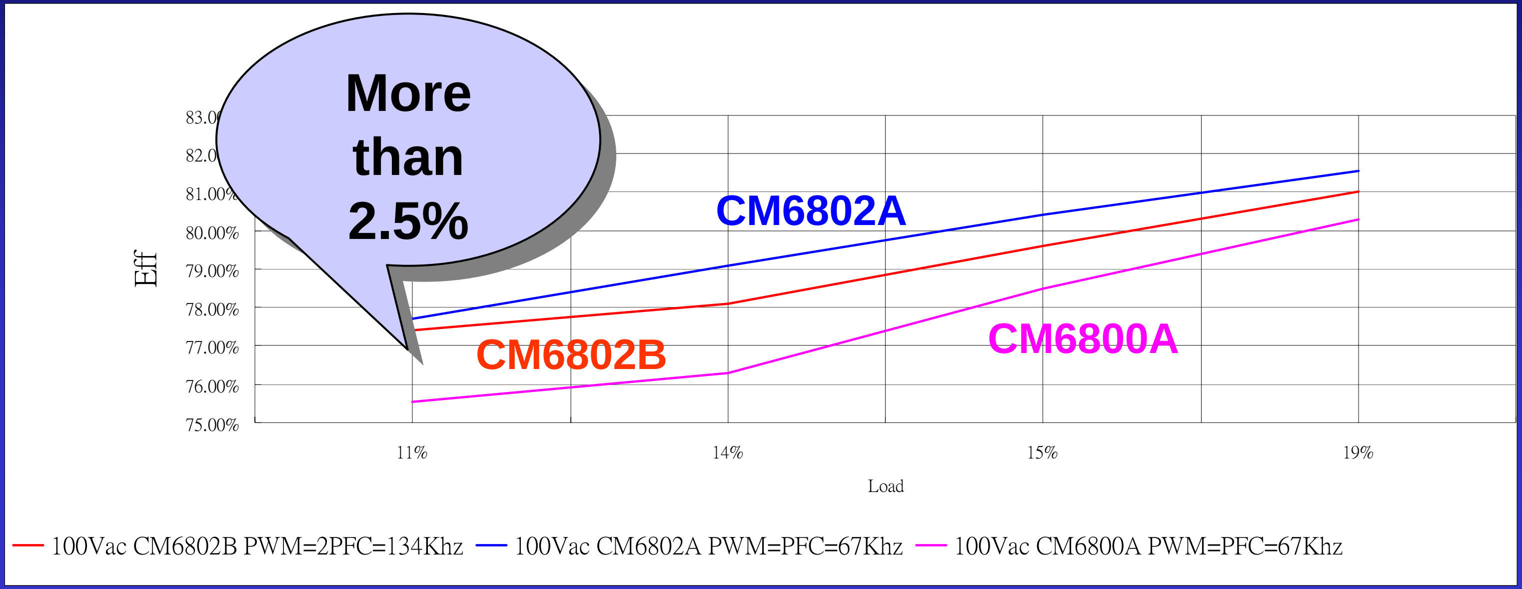


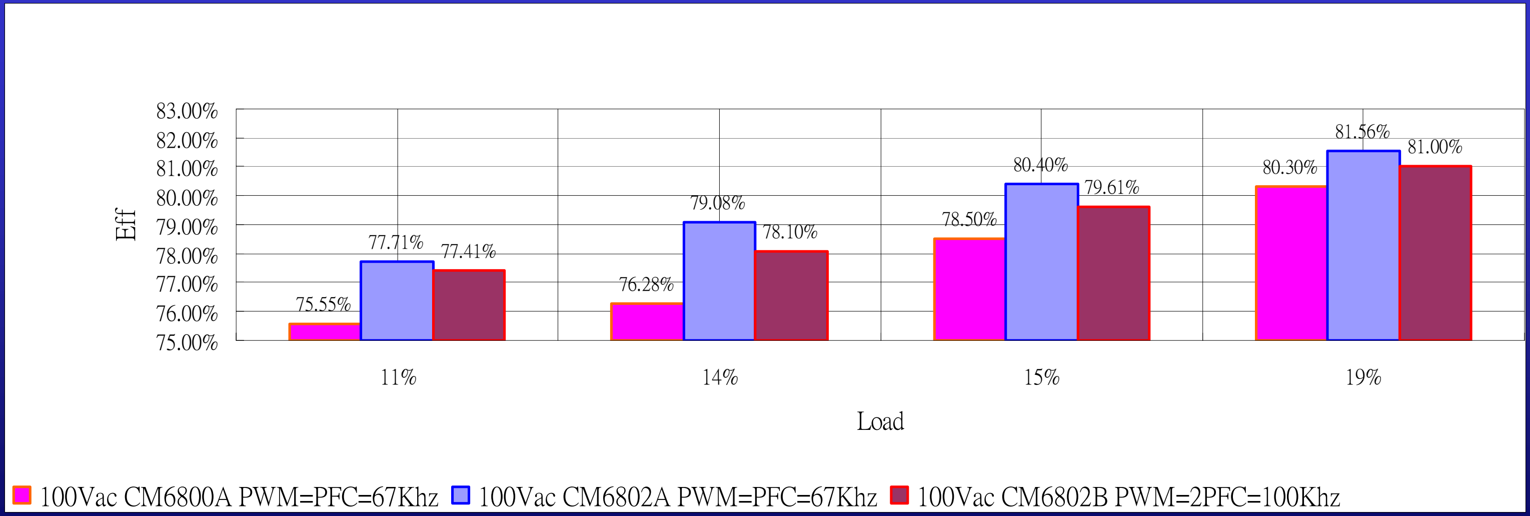
Increase Vin
To reduce Current!

80++ CM6802A


90.00%
85.00%
80.00%
75.00%
70.00%
65.00%
60.00%
Eff
10%
11%
14%
15%
19%
20%
30%
50%
Load
90vac
100Vac
115Vac

CM6800A, CM6802A and CM6802B at light load





80++ CM6802A/B

Dynamic Soft PFC

Reduce PFC Power Device Stress

Just like ZVS without any additional component at fixed switching frequency

Ease EMI filter

- AC Dynamic Brown out
- PWM Brown out
- PFC boost to 380V and 304V
- Ease Monotonic Power Sequence
- Dynamic (Fixed) Switching Frequency

80++ CM6802A/B

Hold-Up Time goes up

3mS to 5mS longer!

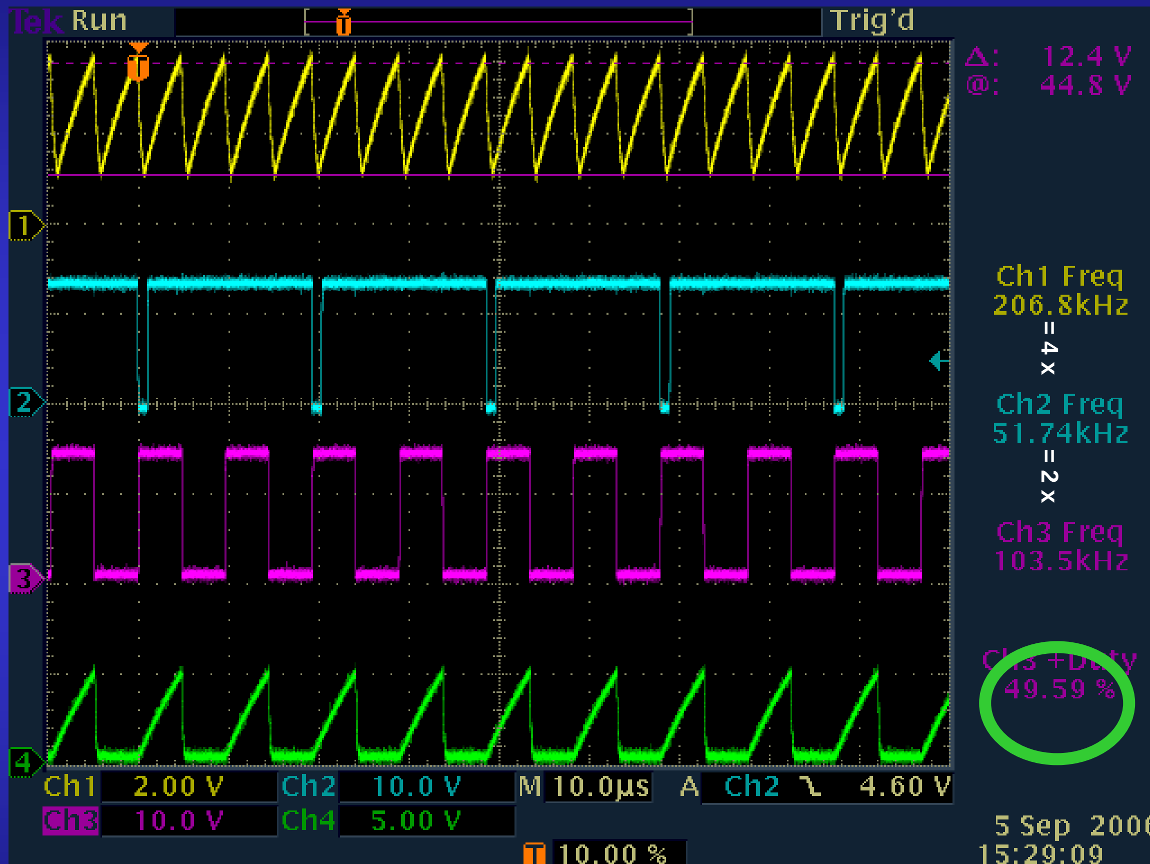
Digitized PWM Maximum Duty Cycle, Dmax

f_{rtct} (pin7)

f_{pfc} (pin12)

f_{pwm} (pin11)

f_{ramp2} (pin8)



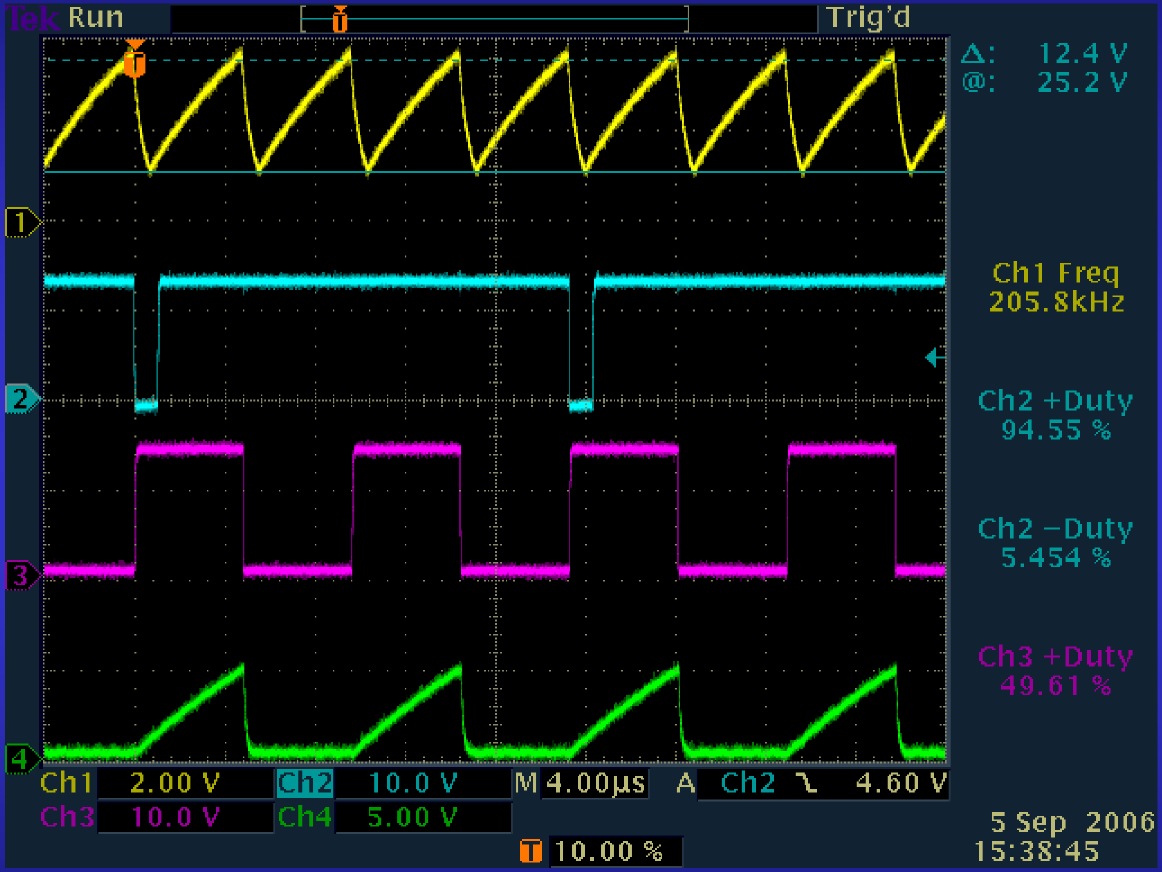
CM6800B Timing Diagram

f_{rtct} (pin7)

f_{pfc} (pin12)

f_{pwm} (pin11)

f_{ramp2} (pin8)



CM6802B Timing Diagram

f_{rtct} (pi

f_{pfc} (pi

f_{pwm} (pi

f_{ramp2} (pin8)

Digitized PWM Dmax = 50%

saving ~ $0.35

for

the Hold-Up time

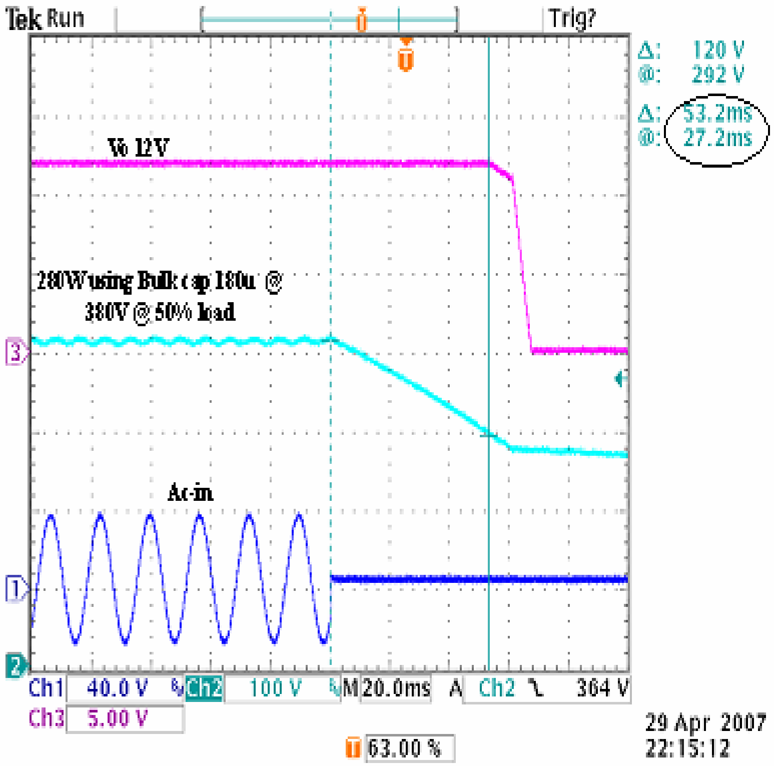
Bulk 450V Cap

CM6802B Timing Diagram

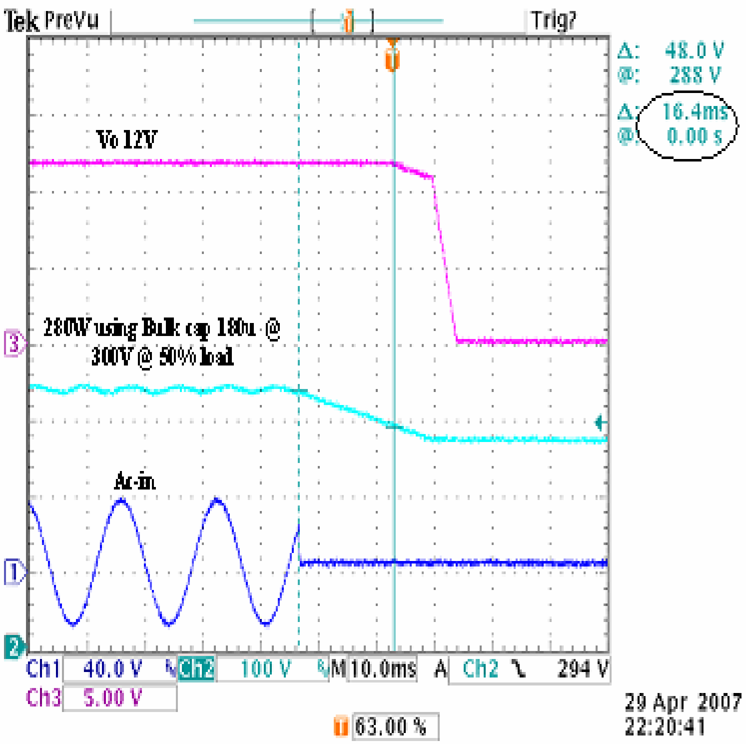
Hold-Up Time @ Vin = 90Vac

Hold up time

90VAC AC-turn off @ 50% load boost voltage = 380V



90VAC AC-turn off @ 50% boost voltage = 300V



80++ CM6802A

f_{rtct}

=

- Leading Edge PFC and Trailing Edge PWM

$4 \times f_{pwm}$

- Higher Efficiency

=

- EMI design easier

$4 \times f_{pfc}$

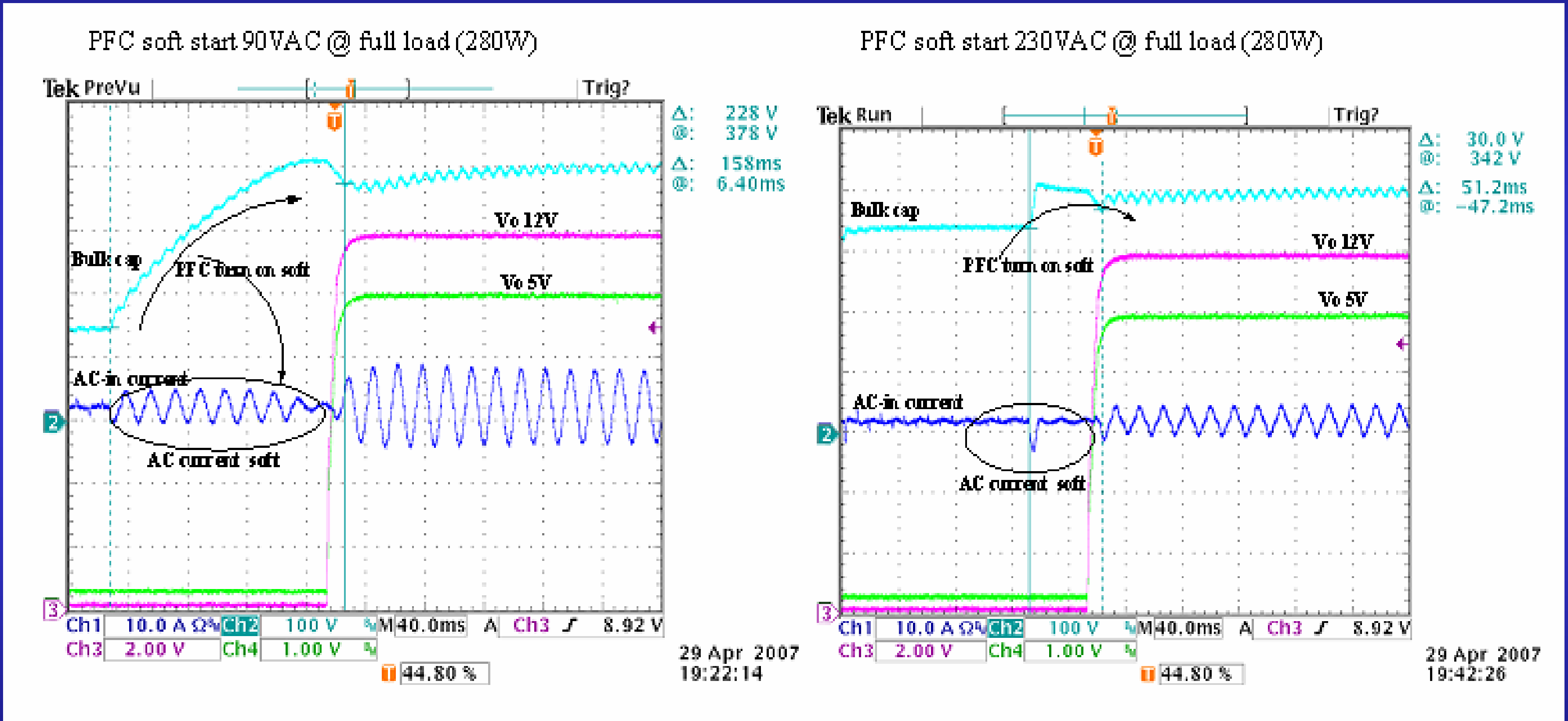
80++ CM6802B

- **Transformer is smaller**
- **Out filters are smaller**
- **3.3V can share the same transformer**

$= 2 \times f_{pwm}$

$= 4 \times f_{pfc}$

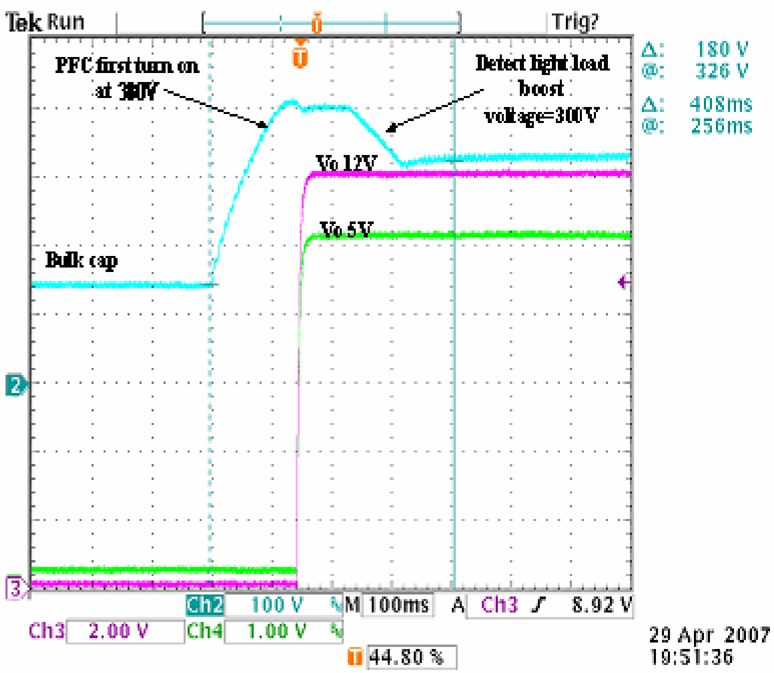
PFC Soft Start @ full load



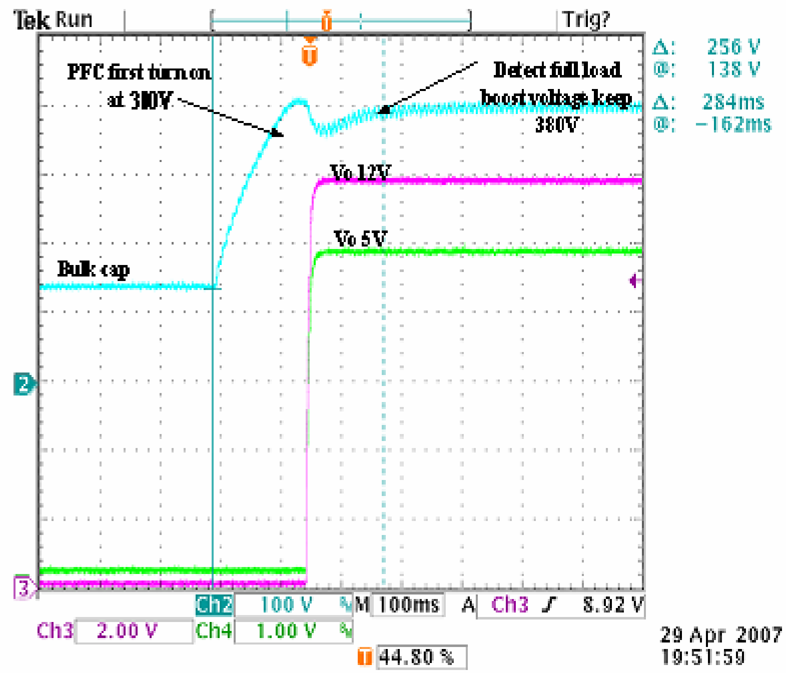
PFC Soft Start @ Vin = 90Vac

380V to 304V function (light load improve efficiency, full load keep hold up time)

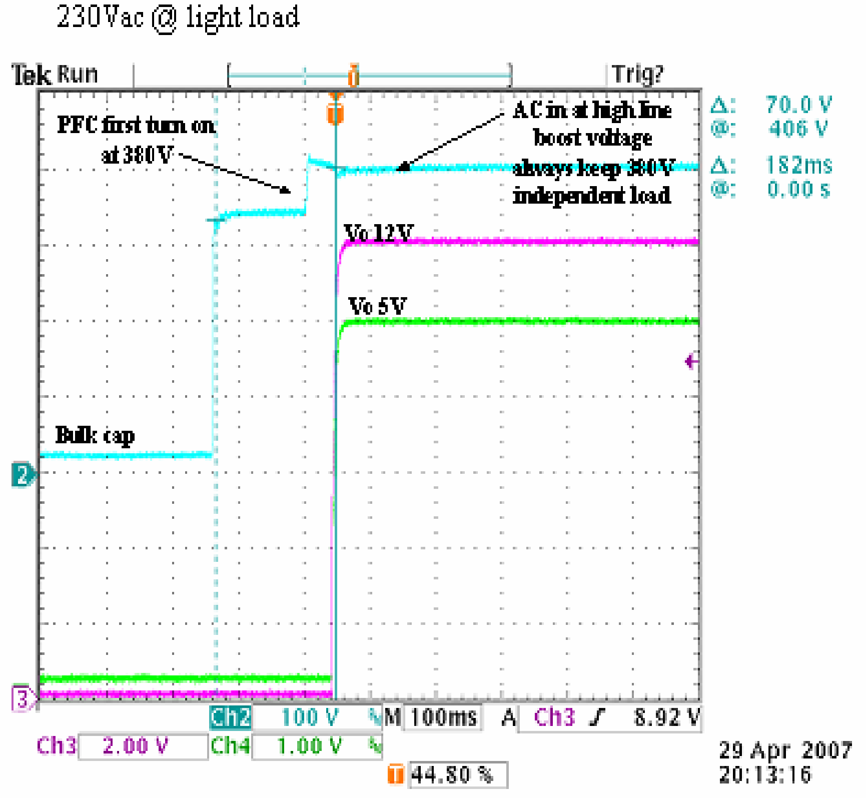
90Vac @ light load

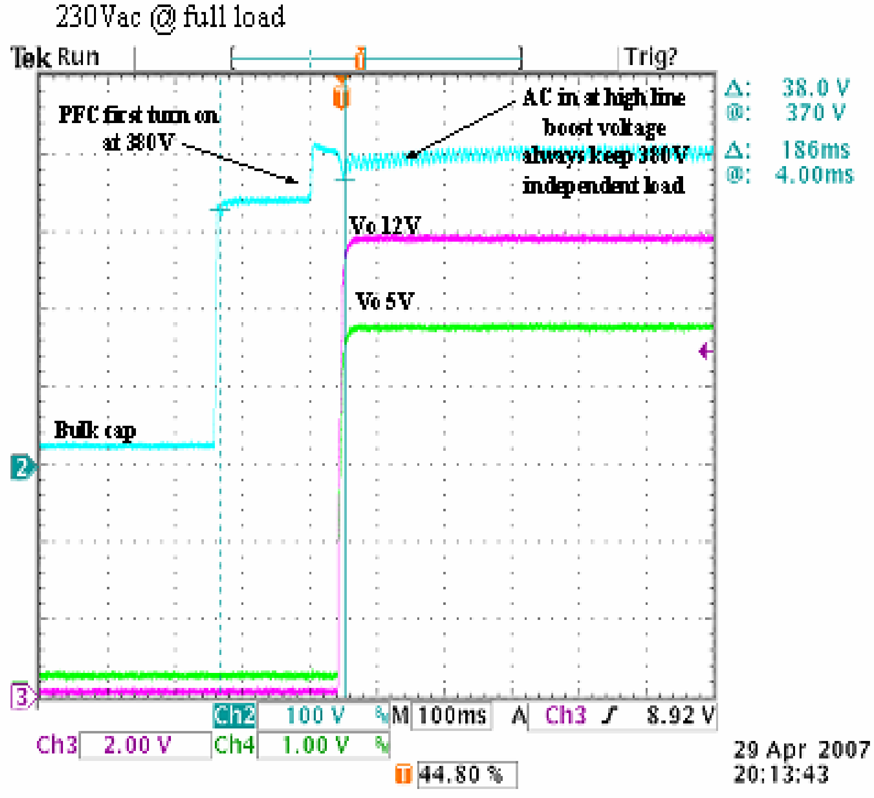


90Vac @ full load

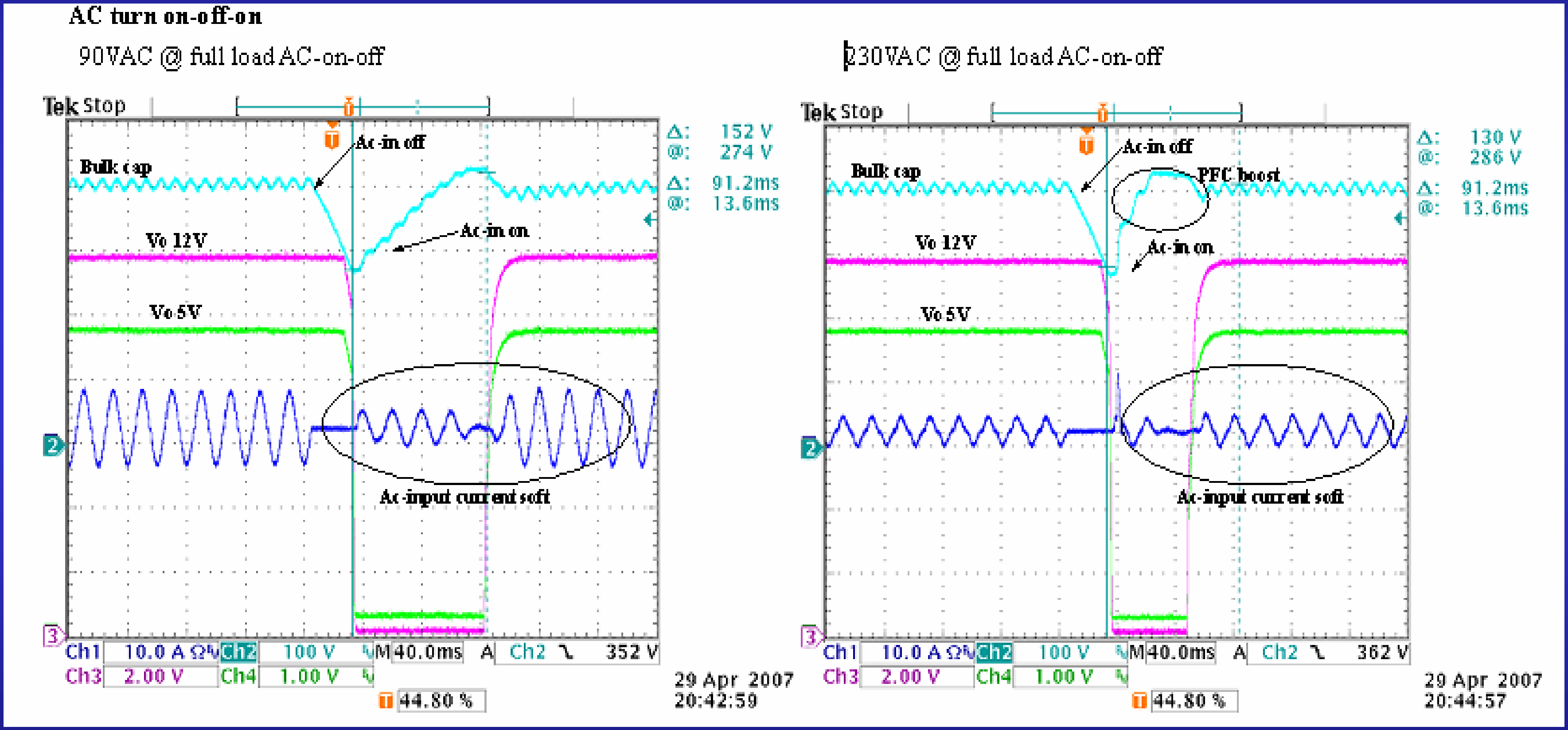


PFC Soft Start @ Vin = 230Vac

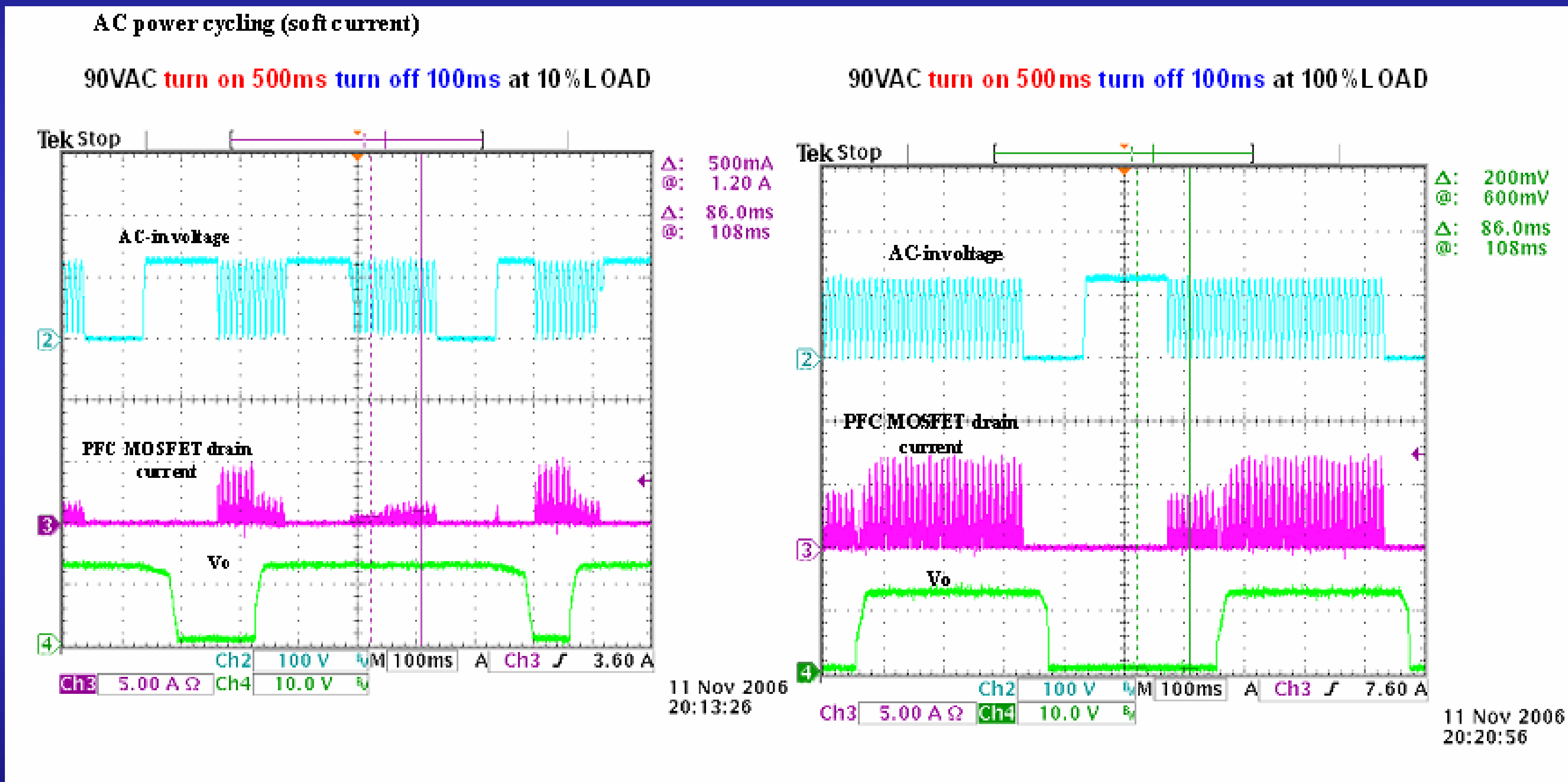




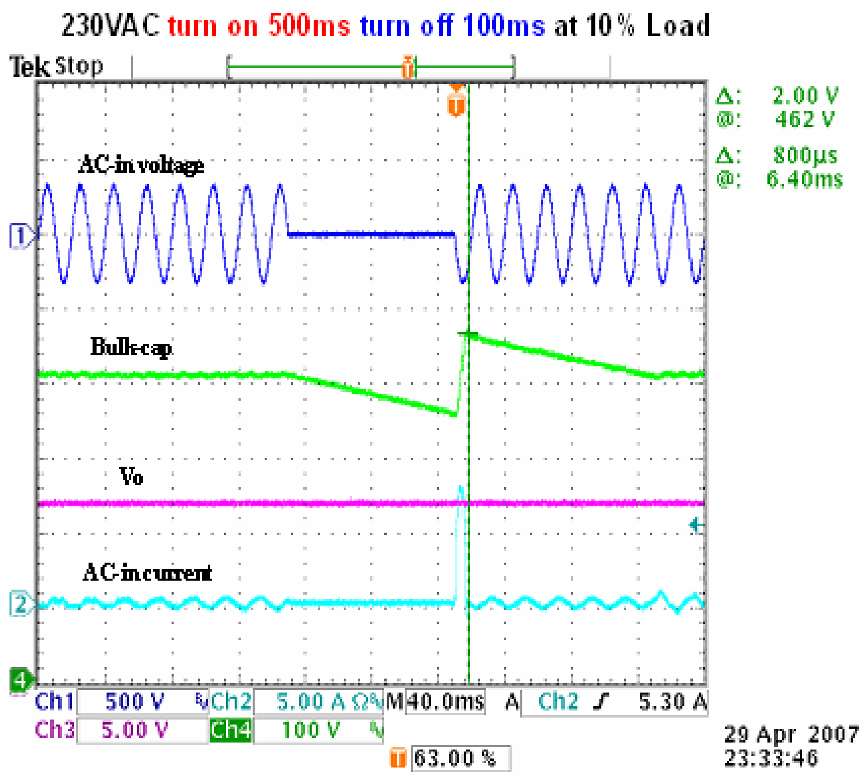
AC On and Off

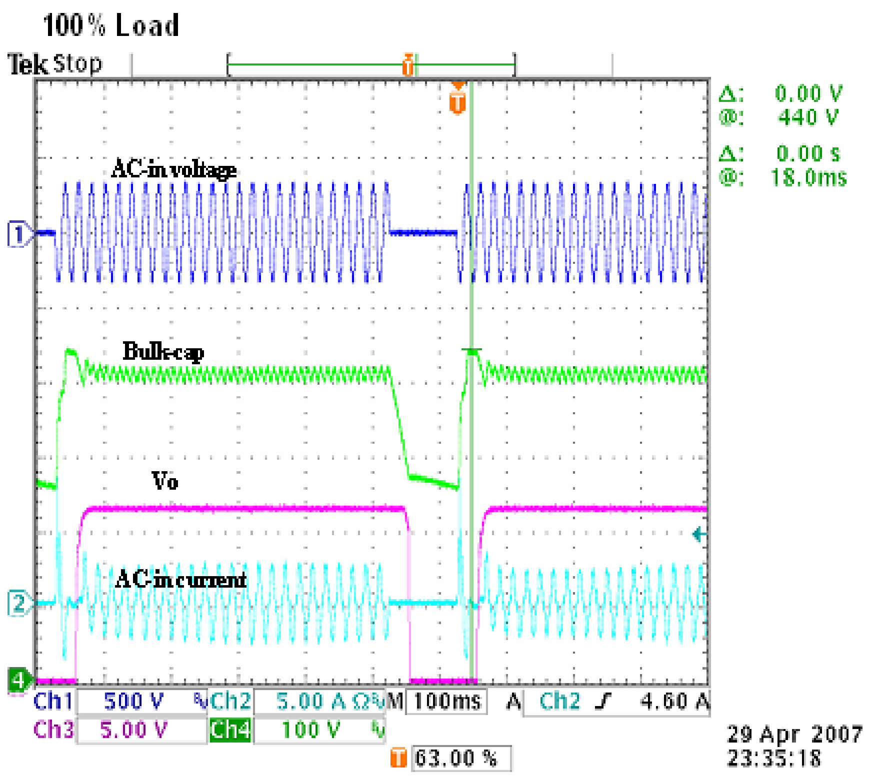

AC turn on-off-on
90VAC @ full load AC-on-off
230VAC @ full load AC-on-off
Tek Stop
Ac-in off
Bulk cap
Ac-in on
Vo 12V
Vo 5V
Ac-input current soft
PFC boost
Δ: 152 V
@: 274 V
Δ: 91.2ms
@: 13.6ms
Δ: 130 V
@: 286 V
Ch1 10.0 A Ω
Ch2 100 V
M 40.0ms
A Ch2 352 V
A Ch2 362 V
Ch3 2.00 V
Ch4 1.00 V
44.80 %
29 Apr 2007
20:42:59
20:44:57

Vin = 90Vac On 500mS / Off 100mS



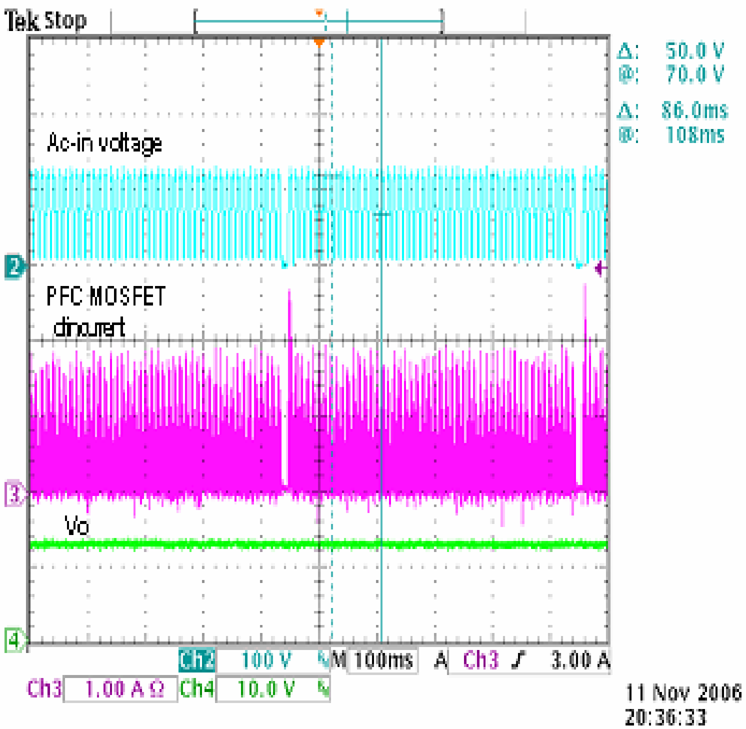
Vin = 230Vac On 500mS / Off 100mS



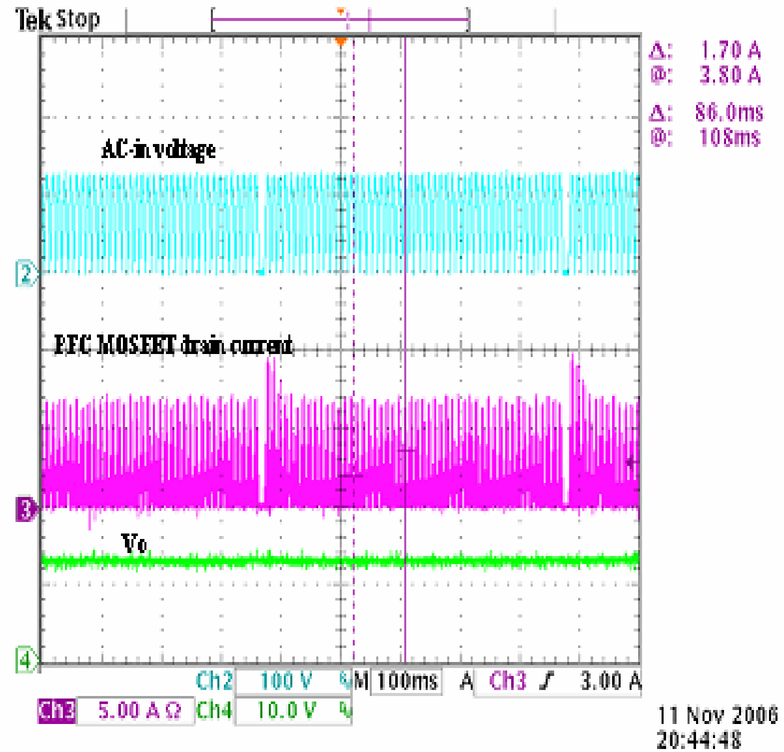


Vin = 90Vac On 500mS / Off 10mS

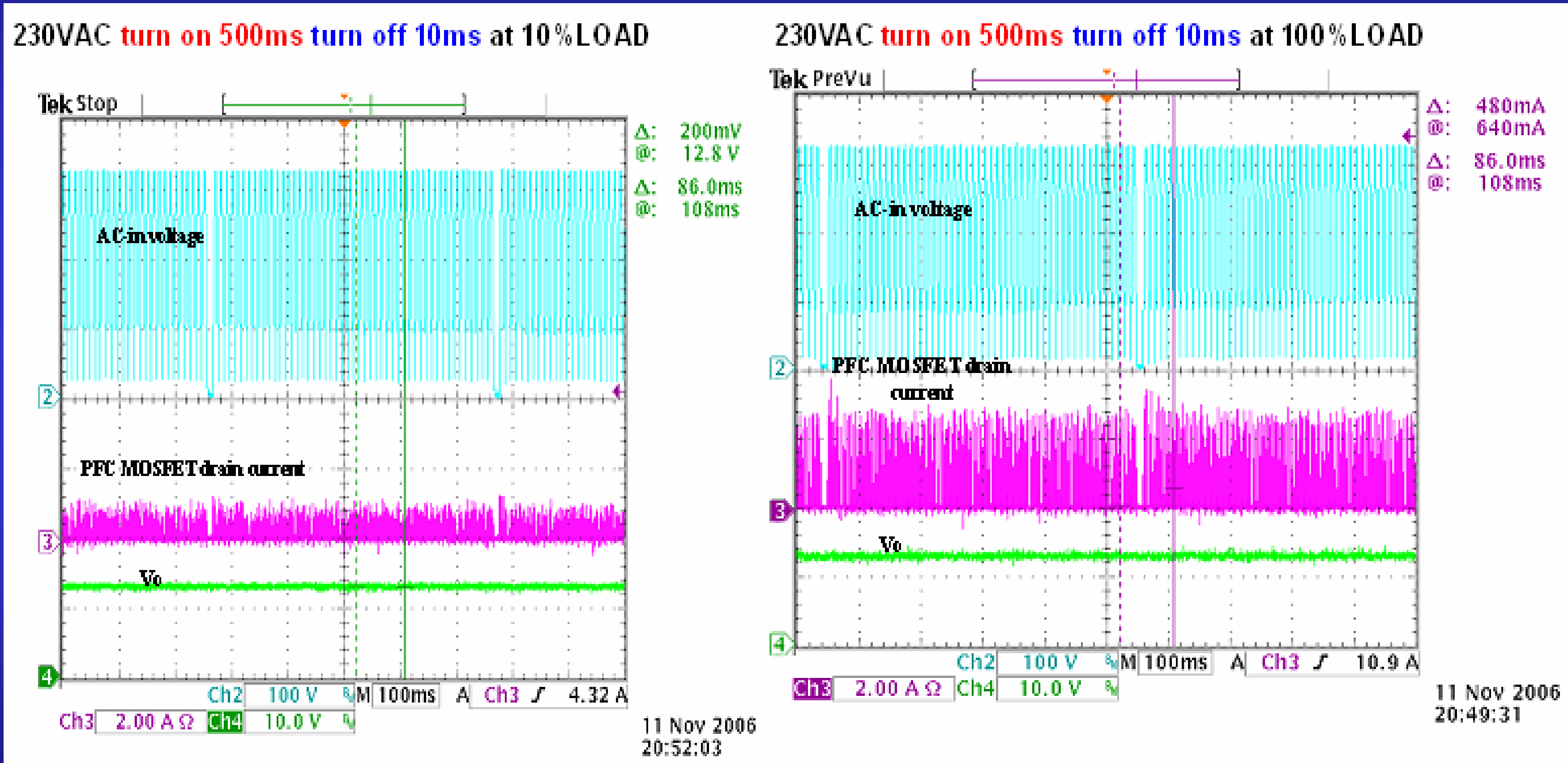
90VAC turn on 500ms turn off 10ms at 10%LOAD



90VAC turn on 500ms turn off 10ms at 100%LOAD



Vin = 230Vac On 500mS / Off 10mS



80++ CM6802A/B

Change all High Voltage

R > 5 Mega Ohm

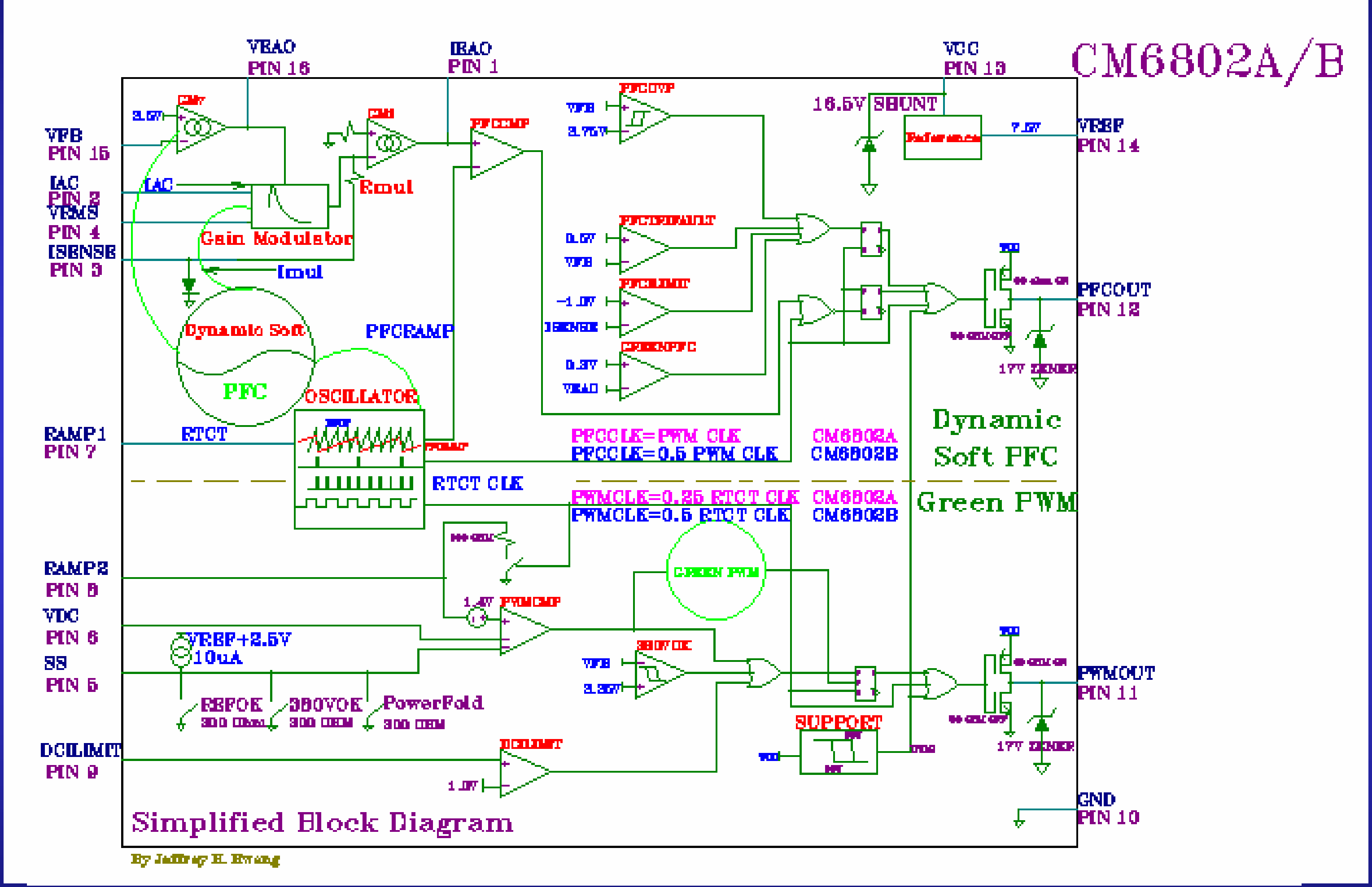
No Load Consumption

Drops

~ 289mW

@ Vin = 264 Vac

Design
High Performance
Power Supply
with
CM6802A/B


CM6802A/B
VEAO
PIN 16
IEAO
PIN 1
VCC
PIN 13
VFB
PIN 15
IAC
PIN 2
VRMS
PIN 4
ISENSE
PIN 3
Rmul
Gain Modulator
Imul
Dynamic Soft
PFC
PFCRAMP
OSCILLATOR
16.5V SHUNT
VREF
PIN 14
PFCOUT
PIN 12
17V ZENER
RAMP1
PIN 7
RTCT
RTCT CLK
PFCCLK=PWM CLK
PFCCLK=0.5 PWM CLK
CM6802A
CM6802B
Dynamic
Soft PFC
Green PWM
PWMCLK=0.25 RTCT CLK
PWMCLK=0.5 RTCT CLK
CM6802A
CM6802B
RAMP2
PIN 8
VDC
PIN 6
SS
PIN 5
VREF+2.5V
10uA
REFOK
380VOK
PowerFold
DCILIMIT
PIN 9
SUPPORT
PWMOUT
PIN 11
17V ZENER
GND
PIN 10
Simplified Block Diagram
By Jeffrey H. Hwang

Convert CM6800/A
to
CM6802A/B

Pin to Pin Compatible with CM6800, FAN4800, ML4800, and ML4824

frtct = 4 x fpfc, pin 7

Vrms level at minimal Vin, pin 4

Rpfcsense at Isense pin, pin 3

Rac at Iac pin, pin 2

Veao level at full load, pin 16

200Khz < frtct = 4 x fpfc < 440Khz; Change rtct @ pin 7

Set Vrms level = 1.125V @ Vin = minimal input

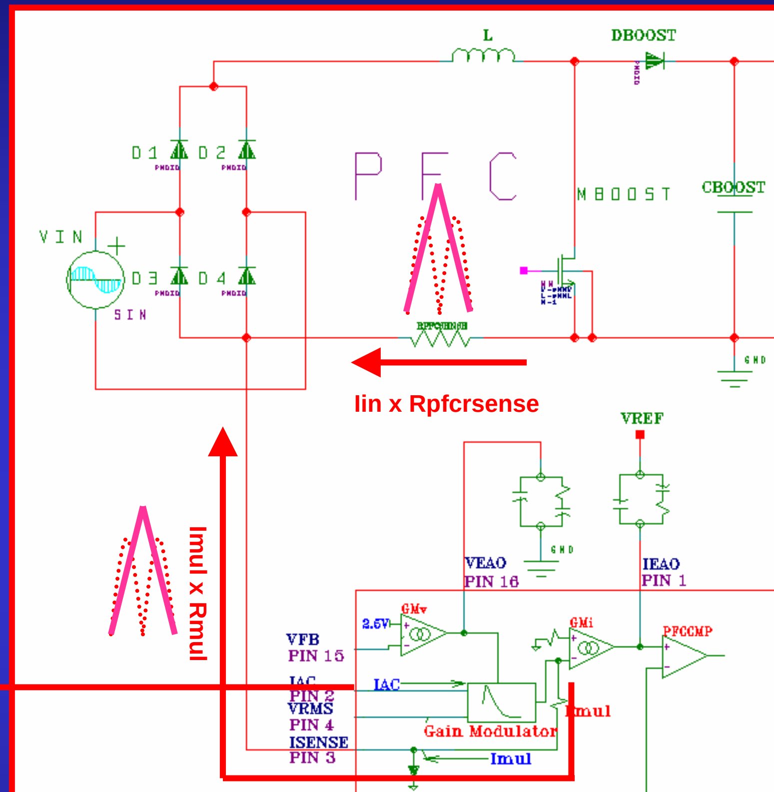
Set Rpfcsense, Imul x Rmul ≤ 0.6V

Start With Rac = 6Mega ohm

Set Veao level ~ 4.5V @ full load & Vin = minimal input

Review the basic PFC

Ieao, GMi forces Iin x Rsense = Imul x Rmul; Therefore,



Rac

Imul ~ 1.19 x Iac x (Veao – 0.7V)/(Vrms x Vrms)

This is the reason that the PFC voltage loop
And
Vrms pin bandwidth is slow and below 30 hz.

* PFC 380V to ... ~ Vref (7.5V)

* Full Input P...

Why need 1/(Vrms x Vrms) in Gain Modulator ??

Iac = (Vin – 1.4V) / Rac

Without 1/(Vrms x Vrms):

Pin = Iin x Vin
→ Pin = (Imul x Rmul / Rpfcsense) x Vin
→ Pin = Iac x (Veao-0.7) x constant1 x Vin
→ Pin = Iac x (Veao-0.7) x constant1 x Vin
→ Pin = [(Vin - 1.4) / Rac] x (Veao-0.7) x constant1 x Vin
→ Pin ~ Vin x Vin x (Veao-0.7) x constant2

Power depends on Veao and Vin x Vin;
Therefore,
both power and bandwidth are not constant.

With 1/(Vrms x Vrms):

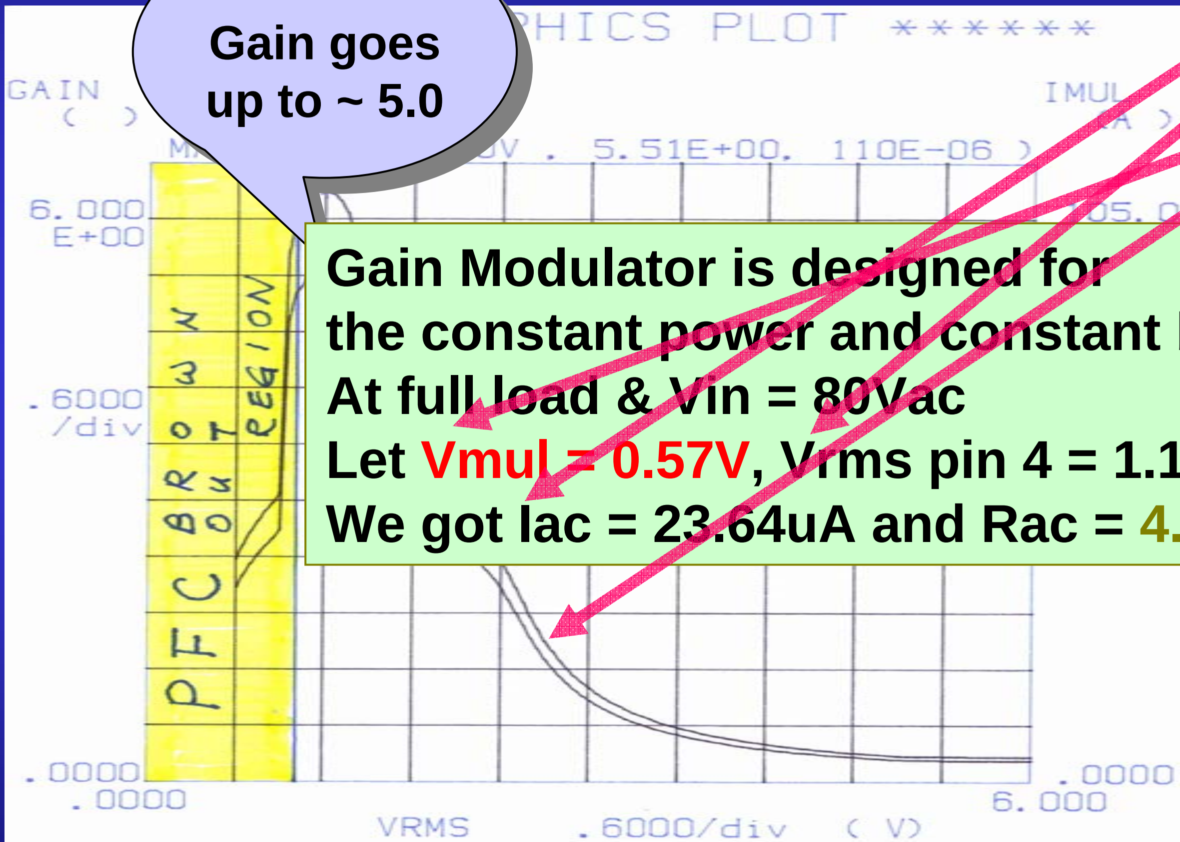
Pin = Iin x Vin
→ Pin = (Imul x Rmul / Rpfcsense) x Vin
→ Pin = Iac x (Veao-0.7) x constant1 x Vin / (Vrms x Vrms)
→ Pin = Iac x (Veao-0.7) x constant1 x Vin / (Vrms x Vrms)
→ Pin = [(Vin - 1.4) / Rac] x (Veao-0.7) x constant1 x Vin / (Vrms x Vrms)
→ Pin ~ Vin x Vin x (Veao-0.7) x constant2 / (Vrms x Vrms)
→ Pin ~ (Veao-0.7) x constant3

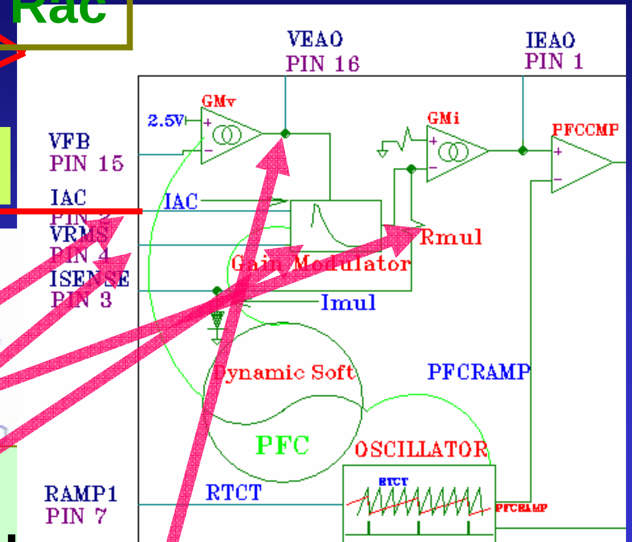
Power depends on Veao only;
Therefore,
both power and bandwidth are constant.

Vrms (pin 4) Gain and Imul

Rac

Gain goes up to ~ 5.0





Gain Modulator is designed for the constant power and constant band width
At full load & Vin = 80Vac
Let Vmul = 0.57V, Vrms pin 4 = 1.125V, Veao = 4V,
We got Iac = 23.64uA and Rac = 4.73 Mega Ohm

Imul ~ 1.19 x Iac x (Veao-0.7) / (Vrms pin 4 x Vrms pin 4)

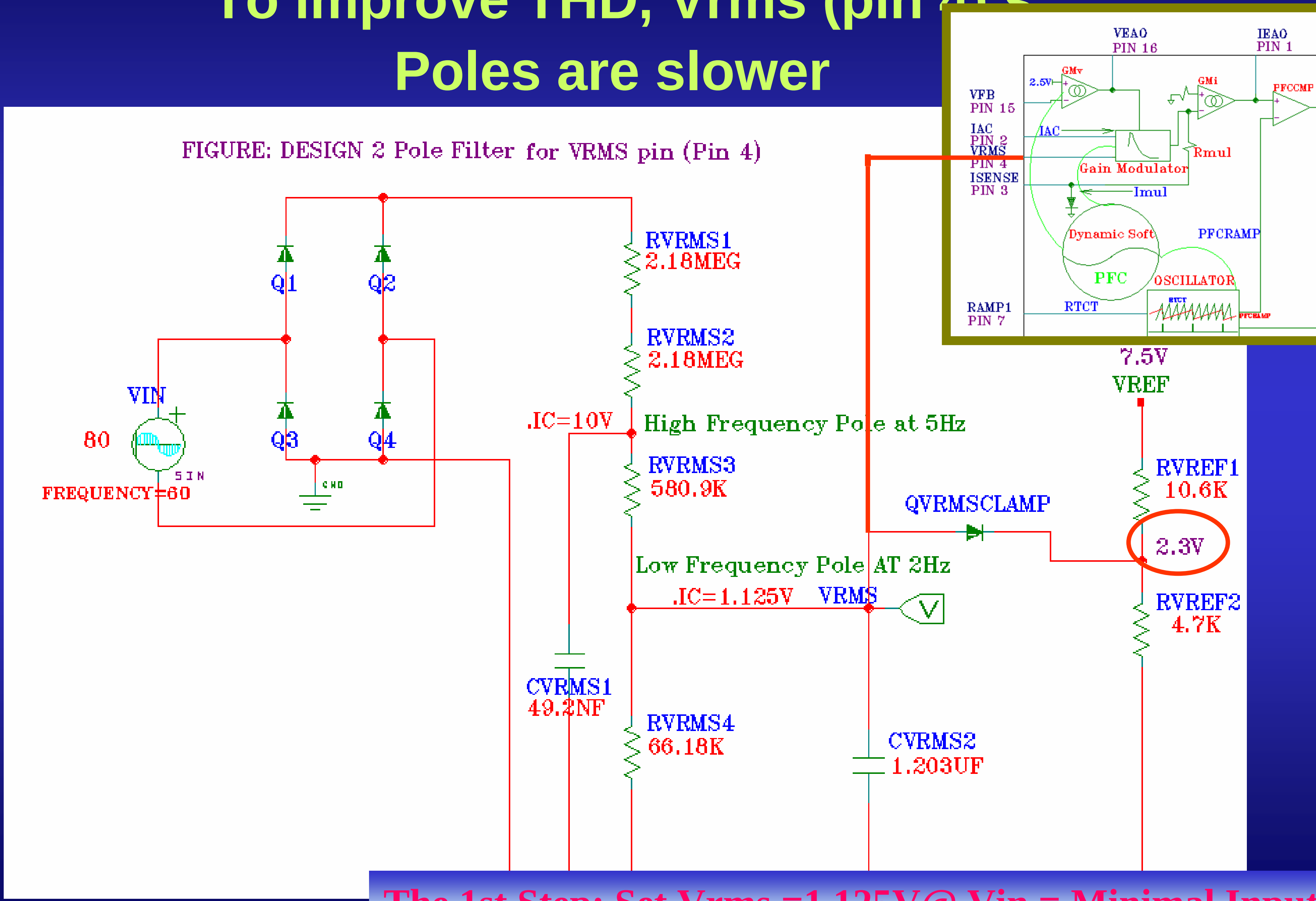
Iac ~ Imul x (Vrms pin 4 x Vrms pin 4) / (1.19 x (Veao -0.7))

~ (Vmul/7.77K) x (Vrms pin 4 x Vrms pin 4) / (1.19 x (Veao -0.7))

IMUL (A) = -(ISENSE+27.5u)

GAIN ( ) = -(ISENSE+27.5u)/IAC

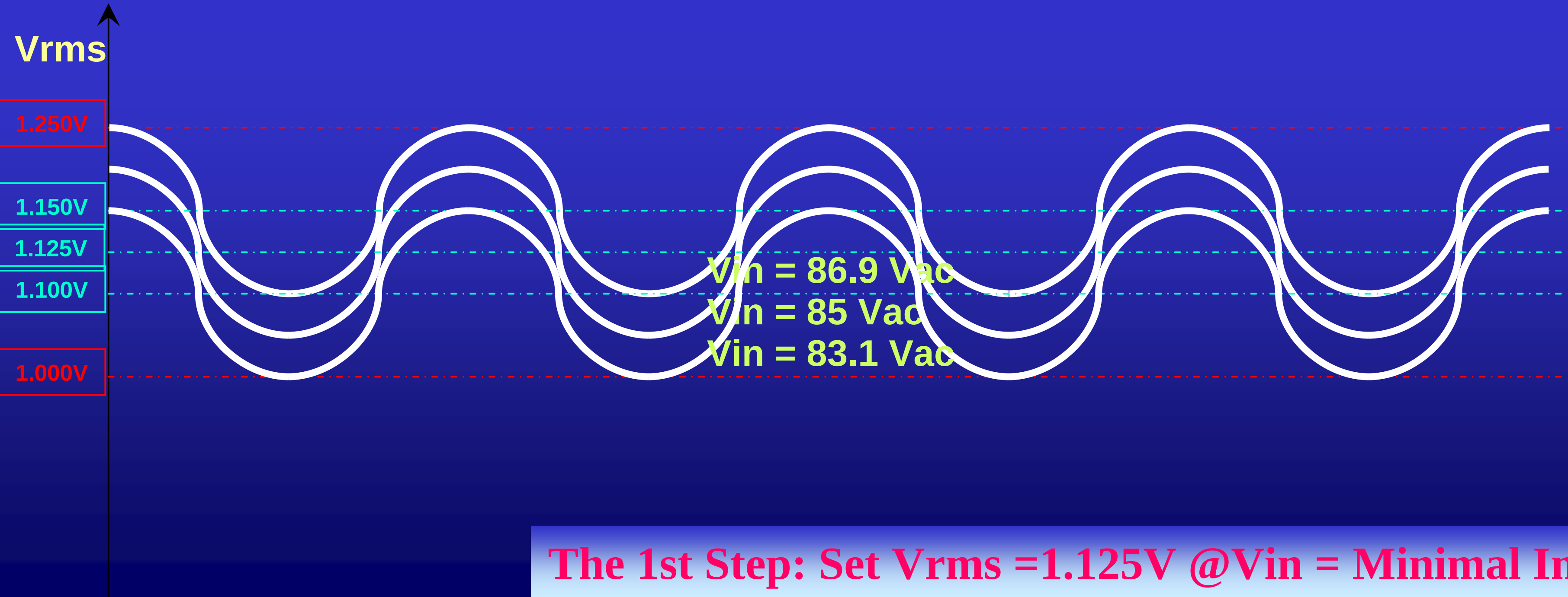
To improve THD, Vrms (pin 4)'s Poles are slower



The 1st Step: Set Vrms =1.125V@ Vin = Minimal Input

Vrms (pin 4)'s AC Brown Out

For CM6802A/B, Vrms resistors' value can be greater than 5 Mega Ohm.
For Vin = 85Vac, Vrms (pin 4) ~ 1.125V
With 100mV p-p, peak to peak ripple, it on at 90.0Vac, and off at 81.2Vac
With 200mV p-p, peak to peak ripple, it on at 86.9Vac, and off at 83.1Vac



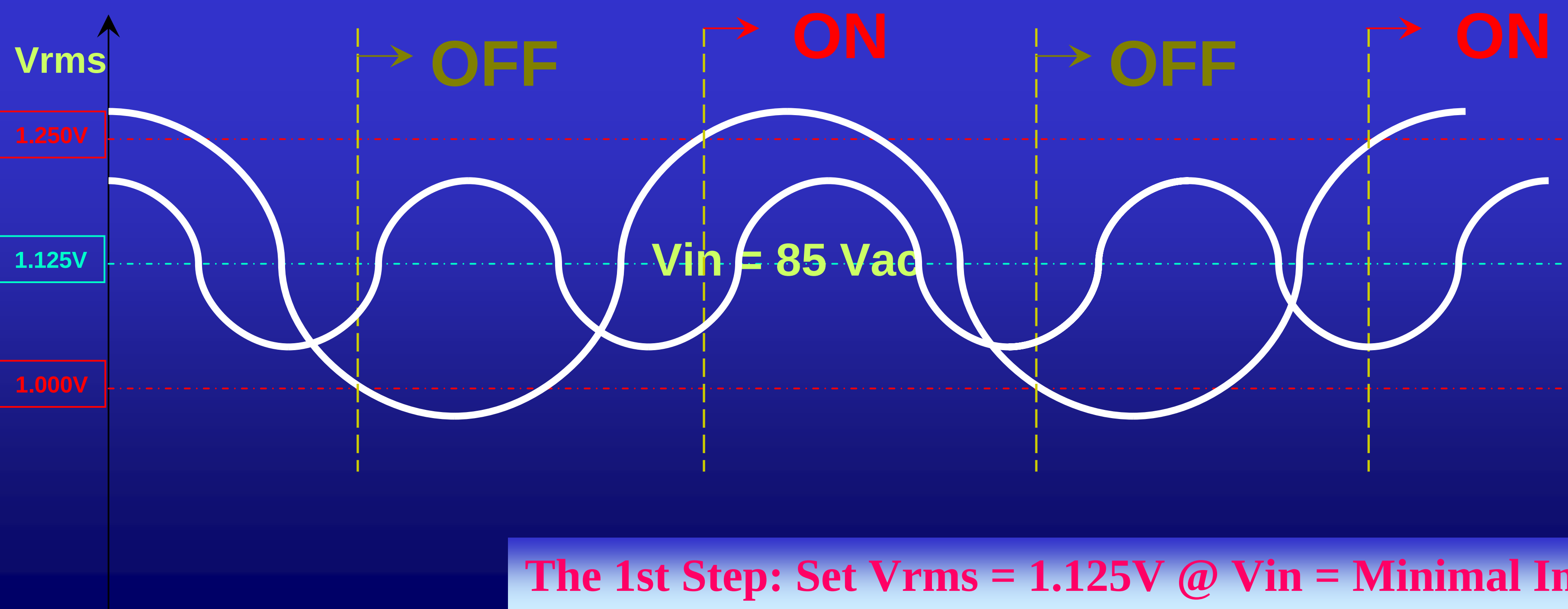
The 1st Step: Set Vrms =1.125V @Vin = Minimal Input

Vrms (pin 4)'s
AC Brown Out

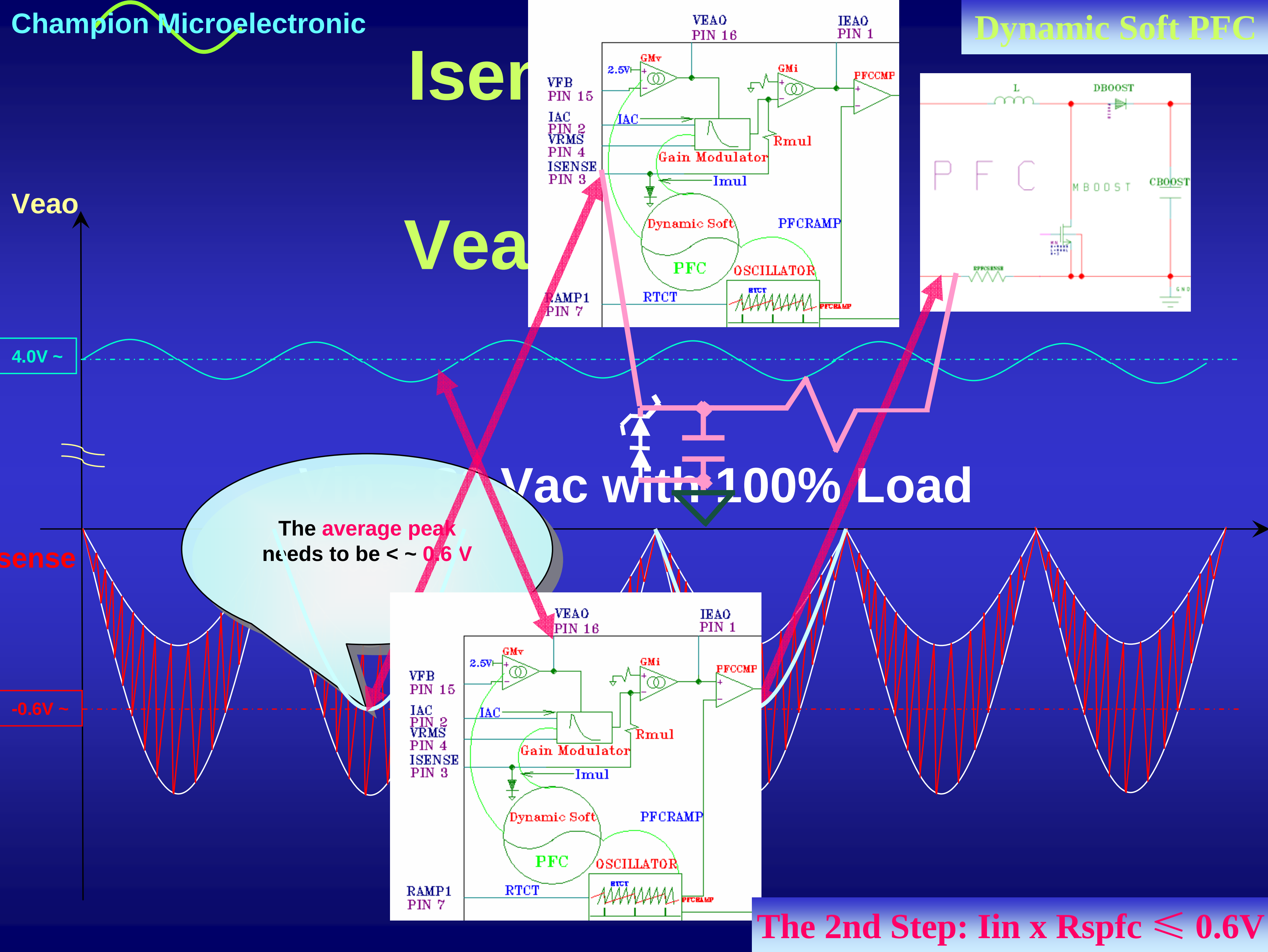
Keep

VRMS AC ripple + Noise less than 250 mV

Avoid VRMS AC ripple + Noise > 250 mV



The 1st Step: Set Vrms = 1.125V @ Vin = Minimal Input



Champion Microelectronic
Dynamic Soft PFC
Isen
Veao
Vea
4.0V ~
Vac with 100% Load
sense
-0.6V ~
The average peak needs to be < ~ 0.6 V
VEAO PIN 16
IEAO PIN 1
GMv
2.5V
GMi
PFCCMP
VFB PIN 15
IAC PIN 2
VRMS PIN 4
ISENSE PIN 3
IAC
Rmul
Gain Modulator
Imul
Dynamic Soft PFC
PFCRAMP
OSCILLATOR
RAMP1 PIN 7
RTCT
L
DBOOST
PFC
MBOOST
CBOOST
The 2nd Step: Iin x Rspfc ≤ 0.6V

80++ CM6802A/B

Rac for Iac (pin 2)

For CM6800, Rac ~ 1 Mega Ohm
For CM6802A/B, Rac can be between 4 Mega Ohm to 6 Mega Ohm

Rac functions:

1. **sense AC input current, IAC current which is the input current of AGC**
2. **It helps to start up CM6802A/B**
3. **Dynamic Soft PFC Input**
4. **Rac value goes up; Power goes down and Veao goes up**
   Rac value goes down; Power goes up and Veao goes down

Need 1nF to Ground at IAC pin for better THD

The 3rd Step: Set Rac so 4V <Veao < 5V @ full load

Review the basic PFC

Ieao, GMi forces Iin x Rsense = Imul x Rmul; Therefore,
Rac Value goes up, ∆Veao goes up … max Power and BW Go down
Rac Value goes down, ∆Veao goes down … max Power and BW Go up
Rsensepfc goes up, ∆Veao goes up … max Power and BW Go down
Rsensepfc goes down, ∆Veao goes down … max Power and BW Go up
Both Rac and Rsensepfc is proportional to ∆Veao

Rsensepfc already has been defined 0.6V ≥ Iin (average peak @ min Vin) x Rsensepfc

Rac = (Vin – 1.4V) / Iac and ∆Veao = Veao – 0.7V

To design Rac: @ Vin = Minimal Vin with full load

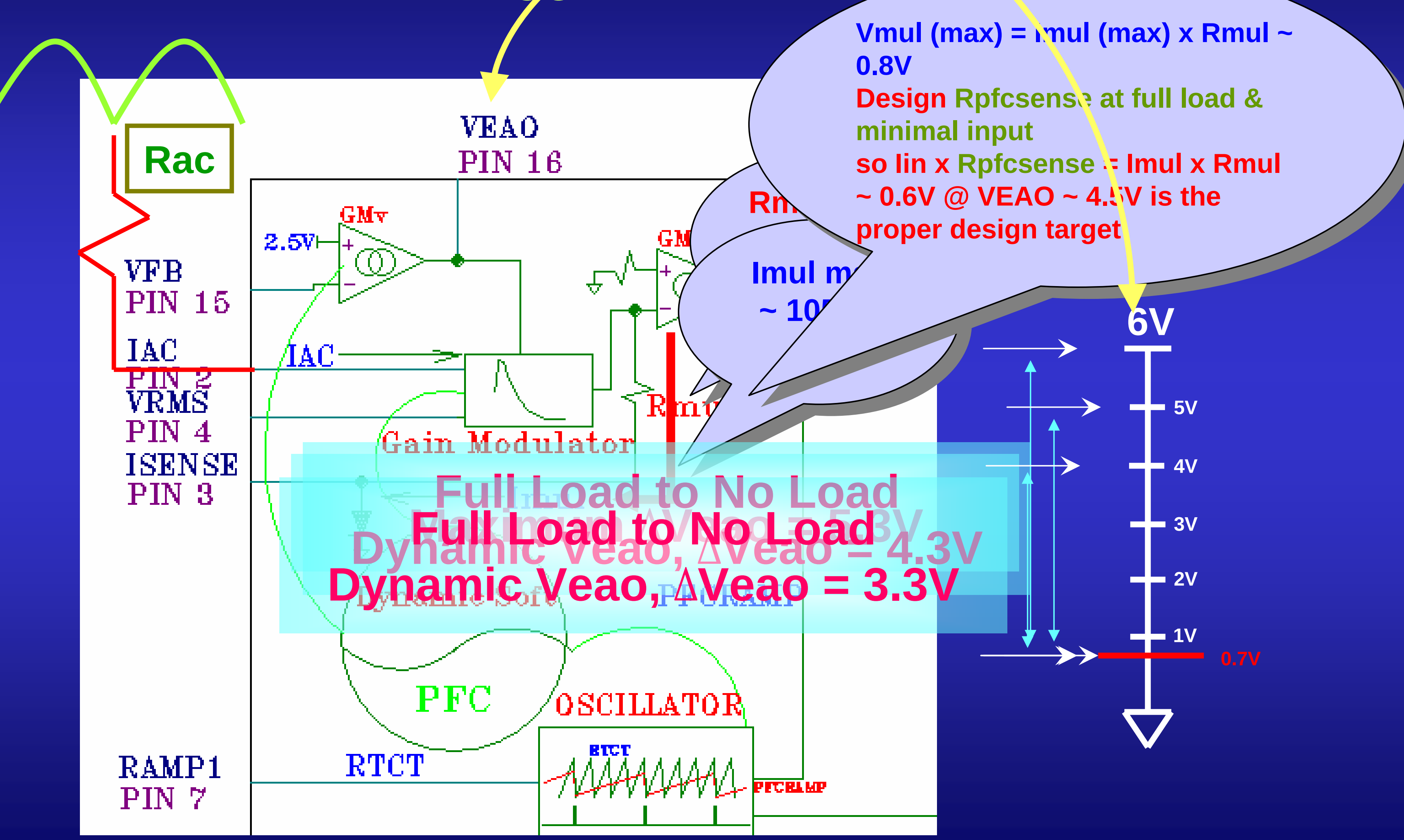
1. Design ∆Veao which usually is between 4V – 0.7V = 3.3V to 5V – 0.7V = 4.3V
2. Iac = (Vin – 1.4V) / Rac
3. Iac ~ Imul x (Vrms pin 4 x Vrms pin 4) / (1.19 x (Veao -0.7))
   ~ (Vmul / 7.77K) x (Vrms pin 4 x Vrms pin 4) / (1.19 x (Veao -0.7))
   = (0.57V / 7.77K) x (1.125V x 1.125V) / (1.19 x (4V -0.7V))
   = 23.6427uA

Therefore, Rac = (Vin - 1.4V) / Iac = (80V x 1.414 - 1.4V) / 23.6427uA = 4.726 Mega Ohm

* PFC 380V to 304V function can be disable by keeping SS (pin 5) below ~ Vref (7.5V)
* Full Input Power: It is the input Power at Full Load

The 3rd Step: Set Rac so 4V <Veao < 5V @ full load

Rac ~ 4.7 Mega Ohm for Min Vin = 80Vac



Minimal Capacitor Value Design for PFC 380V to 304V and Hold Up Time Design

DC to DC PWM brown out threshold (VINOK) high at Vfb is 2.365V which represents 359V.
DC to DC PWM brown out threshold (VINOK) low at Vfb is 1.5V which represents 228V.

$$\frac{(380V \times 380V - 228V \times 228V)}{(304V \times 304V - 228V \times 228V)} = \frac{(92.416\ E3)}{(40.432\ E3)} = 2.2857 = 1/0.437$$

Above Information tells us to get the minimal bulk capacitor value design for Hold Up Time, PWM Duty Cycle should be 30% when bulk voltage is 380V and PWM Duty Cycle should be 50% when bulk voltage is 228V.

If the efficiency curve is constant, full load and light load to have the same hold up time, the minimal light load for PFC goes back to 380V is 43.7% load.
If the efficiency at 50% load is higher, it could be OK to wait until 50% load for PFC goes back to 380V.

* PFC 380V to 304V function can be disable by keeping SS (pin 5) below ~ Vref (7.5V)

Adjust Rac value to
Design Veao Voltage, ΔVeao = Veao – 0.7V

When Vrms is < ~ 2.0V (low line, Vin ~ 142Vac) and Veao is < ~ 1.75V, PFC 380V drops to 304V.

When Vrms is > ~ 2.5V (high line, Vin ~ 178Vac) or Veao is > ~ 2.5V, PFC 304V raise to 380V.

Increase Rac, Power goes down and ΔVeao goes up.
Reduce Rac, Power goes up and Δ Veao goes down.

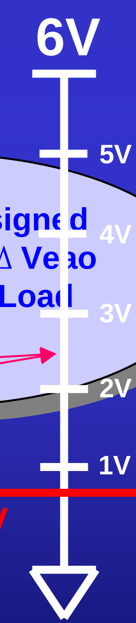
Since the Gain Modulator keep PFC power and band width constant, we can assume Veao is pretty linear with input power.

Let Veao is 2.5V when it is 43.7% input power
Then at full input power, Veao is (2.5V - 0.7V) / (43.7%) + 0.7V = 4.8V
Let Veao is 2.5V when it is 50% input power.
Then at full input power, Veao is (2.5V - 0.7V) / (50%) + 0.7V = 4.3V
Therefore, the formula is (2.5V- 0.7V) / load% + 0.7V = Designed Veao Voltage, Δ Veao +0.7V

This is the designed % of Full Input Power goes back to 380V

This is the Designed Veao Voltage , Δ Veao ull Load

100%



* PFC 380V to 304V function can be disable by k
* Full Input Power: It is the input Power at Full L

The 3rd Step: Set Rac so 4V <Veao < 5V @ full load

Adjust Rac value to
Design Veao Voltage, ΔVeao = Veao – 0.7V

The Voltage Loop Gain (S)

$$=(\Delta Vout/ \Delta Veao) \times (\Delta Vfb/ \Delta Vout) \times (\Delta Veao/ \Delta Vfb)$$

$$\sim (Pin \times 2.5V \times GMv \times Zcv)/(380V \times 380V \times \Delta Veao \times S \times Cdc)$$

Z_{CV}: **Compensation Net Work for the Voltage Loop**
GM_{V}: **Transconductance of VEAO typical ~ 72 mho**
P_{IN}: **Average PFC Input Power**
V_{OUTDC}: **PFC Boost Output Voltage; typical designed value is 380V.**
C_{DC}: **PFC Boost Output Capacitor**
ΔVeao: The maximum value is 6V-0.7V=5.3V
2.5V: It is the input reference of the GMv.

* PFC 380V to 304V function can be disable by k
* Full Input Power: It is the input Power at Full L

The 3rd Step: Set Rac so 4V <Veao < 5V @ full load

80++

CM6802A/B

1

2.

Change all high V n

Resistors > 5 Mega Ohm

so so Veao average < 4.5V

Performance Gain

	Saving
1. Efficiency Goes up ~ 1.5% to 2%	US$???
2. Electrical Stress on the Power Device Reduced	US$ 0.25
3. Hold-Up time goes up 3mS to 5mS	US$ 0.35
4. EMI filter is easy	US$???
5. Monotonic Output is easy	US$???
6. No Load Consumption Drops ~ 0.3 W	US$???

Total Saving greater than US$ 0.60

CM6802A/B

Better Efficiency, Ease Design, Lower BOM Cost

There are more goodies for you to find out

More features and benefits!