

CM6800 compensation rule Championmicro-Elvis Lin -July-2004

圖 1 為 CM6800 架構圖，以下將針對 CM6800 將其電壓迴路(voltage loop)與電流迴路(current loop)的應用討論如下：

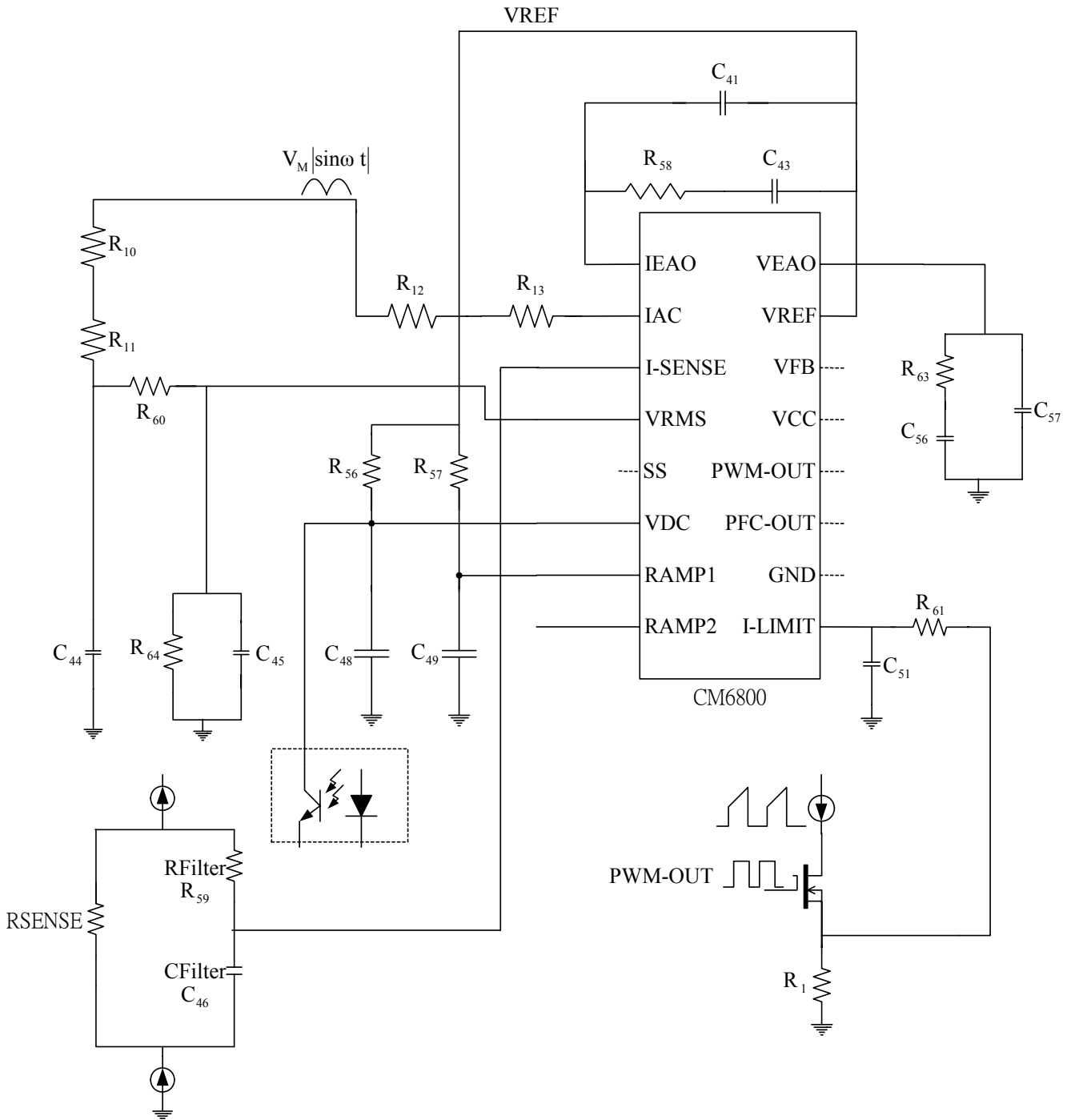


圖 1 CM6800 架構圖

(A)RAC :

RAC 為 gain modulator 的輸入，做為參考訊號，此電阻值的設定為 $RAC = v_{in_PEAK} \times 10$ 以輸入電壓為 80rms，RAC 的值約為 $80 \times \sqrt{2} \times 10 \approx 1M\Omega$ 。

(B)Isense :

Isense 訊號為當 boost converter 在開關切換動作時所流過的電流再乘上 RSENSE，經過一 low-pass filter 後送入 IC， R_{Filter} 的選擇，一般選擇 R_{Filter} 為 $47\Omega \sim 200\Omega$ ，因 Isense 之訊號需 filter (note1) 為 $\frac{1}{6} \sim \frac{1}{10}$ switching frequency(f_s)，故可決定 C_{Filter} 。

note1 :

$$Isense_{frequency} = \frac{1}{2\pi \times R_{Filter} \times C_{Filter}}$$

(C)VRMS :

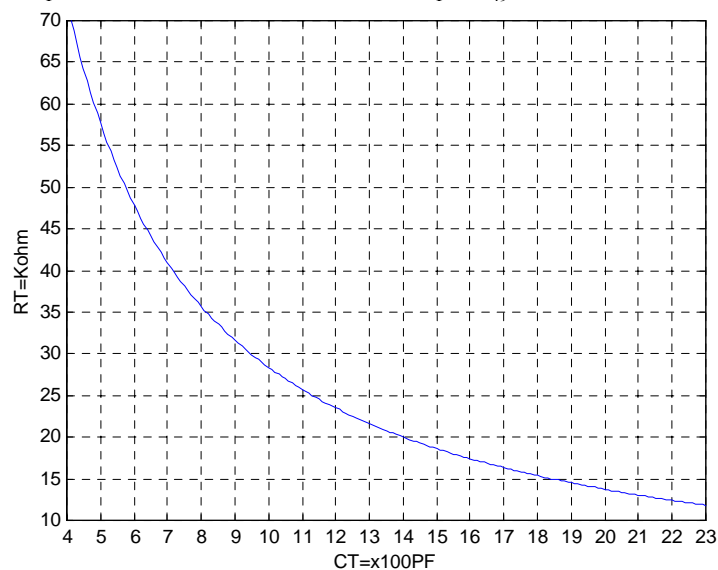
VRMS，為橋式整流端經開關切換後的信號，再經過 2 階低通濾波器電路送入 IC 作為 A.G.C 之 input，在此設定 VRMS 電壓為 $1.1V(80v_{ac})$ 。

(D)RAMP1(R_T & C_T)的選擇 :

在 CM6800 中 C_T 建議值為 $200PF \sim 1000PF$ ，其振盪頻率為：

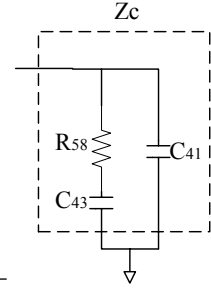
$$f_{osc} = \frac{1}{(t_{RAMP} + t_{DEADTIME})} = 67K_{HZ}, t_{RAMP} = C_T \times R_T \times \ln \frac{V_{REF} - 1.25}{V_{REF} - 7.25}, V_{REF} = 7.5V = C_T \times R_T \times 0.51$$
$$t_{DEADTIME} = \frac{2.5V}{5.5mA} \times C_T = 454.5 \times C_T$$

利用式(1)-(3)可求出 R_T 與 C_T 曲線，如圖 2，在此選用 $C_T (C_{49}) = 470 PF$ 與 $R_T (R_{57}) = 53.6K\Omega$ 。



fig(2) R_T 與 C_T 曲線

NOTE : zero-pole net-work



$$Z_{Cl} = (R_{58} + \frac{1}{SC_{43}}) // \frac{1}{SC_{41}} = \frac{\frac{SR_{58}C_{43} + 1}{SC_{43}SC_{41}}}{\frac{SR_{58}C_{43} + 1}{SC_{43}} + \frac{1}{SC_{41}}} = \frac{SR_{58}C_{43} + 1}{S^2R_{58}C_{43}C_{41} + S(C_{43} + C_{41})}$$

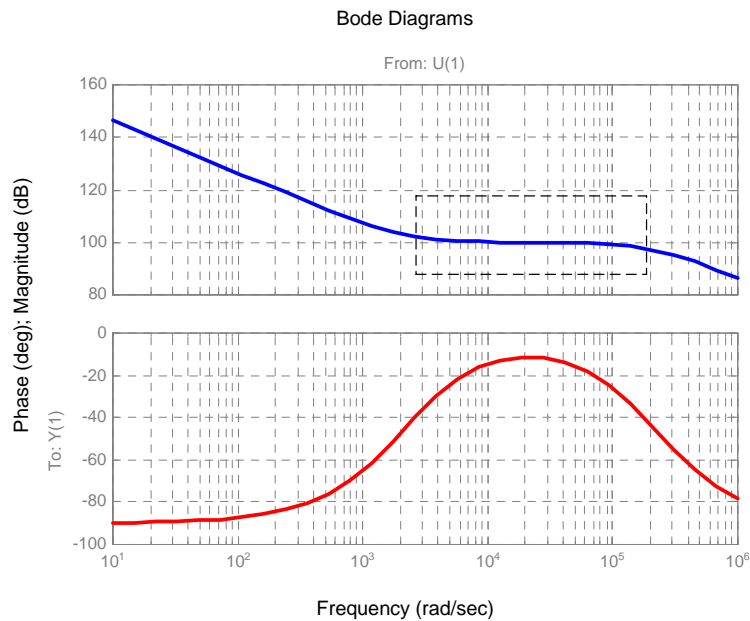
$$= \frac{SR_{58}C_{43} + 1}{S(C_{43} + C_{41})(S\frac{R_{58}C_{43}C_{41}}{C_{43} + C_{41}} + 1)}$$

assume $C_{43} \gg C_{41}$ 由式(9)可知 $Z_{Cl} \approx \frac{SR_{58}C_{43} + 1}{SC_{43}(S\frac{R_{58}C_{43}C_{41}}{C_{43}} + 1)} = \frac{SR_{58}C_{43} + 1}{SC_{43}(SR_{58}C_{41} + 1)}$

有 2 個 pole 和一個 zero 其中 pole 的位置在 $S = 0$ 和 $S = -\frac{1}{R_{58}C_{41}}$ ，zero 的位置在 $S = -\frac{1}{R_{58}C_{43}}$ ，由

假設條件($C_{43} \gg C_{41}$)可知系統一開始有一個 pole 在 $S = 0$ 以此時以 -20db/dec 的 slope 下降，頻率增加遇到 zero， $S = -\frac{1}{R_{58}C_{43}}$ ，此時 slope=0，同時可得到一段平坦的增益，頻率再增加遇到 pole，

$S = -\frac{1}{R_{58}C_{43}}$ ，以 -20db/dec 的 slope 下降，其波德圖可表示如下：



Z_{Cl} 頻率響應圖

由圖可知，在圖中的平坦增益近似 R_{58} ，由以上的分析，即可設計系統所需的 pole 與 zero 的位置

與增益的大小。

(E)IEAO :

IEAO 的補償為 GM_i 乘上 zero-pole network，一般選擇其 unity-gain 為 $\frac{1}{6}$ switching-frequency = 23.33KHz，zero 的位置為 0.1pole。

Example : current loop design

$$\text{Loop gain of the current loop} = \frac{V_o \times R_{\text{SENSE}}}{SLV_{R_T C_T P-P}} \times GM_i \times Z_{C_i} \quad (0)$$

note:

G_{mi} : current loop error amplifier's transconductance，CM6800=100 μ ($\frac{1}{\Omega}$)

Z_{C_i} : compensation net-work

V_{out} : PFC boost converter output voltage

f_c : unity gain frequency, usually set $\frac{f_s}{6}$ = 11.166KHz (switching frequency),

set unity gain frequency at 11.166KHz, from equation (0) we can obtain equation (1).

$$1 = \frac{V_o \times R_{\text{SENSE}}}{SLV_{R_T C_T P-P}} \times GM_i \times Z_{C_i}, \text{ at } 11.166\text{KHz} \quad (1)$$

從式(1), 可求得 Z_{C_i}

$$\begin{aligned} GM_i \times Z_{C_i} &= \frac{SLV_{R_T C_T P-P}}{V_o \times R_{\text{SENSE}}} \\ &= \frac{2 \times \pi \times 11.166\text{K}_{\text{HZ}} \times 737.2987\mu\text{3} \times 2.5}{380 \times 0.09} \approx GM_i \times R_{58} \end{aligned} \quad (2)$$

note:

V_{out} =380V

L = 735.2987 μ H

G_{Mi} = 100 μ mho

$V_{R_T C_T P-P}$ = 2.5V

Set R_{SENSE} = 0.09 Ω

Using equation (2), R_{58} is

$$R_{58} \approx 20\text{K}\Omega \quad \text{at} \quad G_{Mi} = 100\mu \text{ mho}$$

using unity gain frequency at 11.166KHz (f_c), $f_c = 11.166\text{KHz} \approx \frac{1}{2 \times \pi \times R_{58} \times C_{41}}$, therefore

$R_{58} = 20K\Omega$ $C_{41} = 347.878PF$, Let the zero=0.1 pole, therefore $C_{43} = 10 C_{41}$

current loop compensation

current loop for leading edge modulation PFC , leading edge 可表示成圖 1

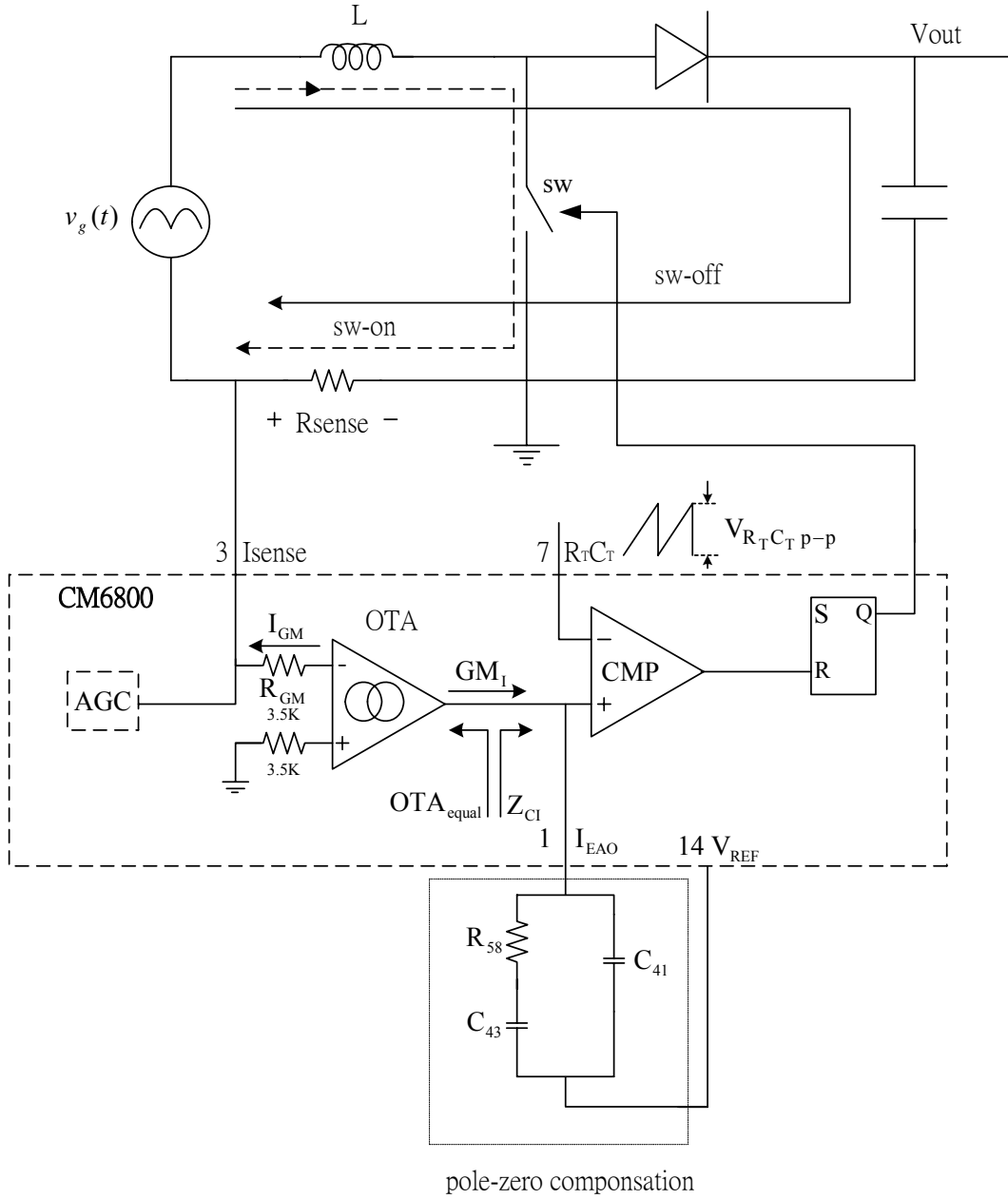


圖 1 PFC leading edge

current loop gain define :

$$\frac{\Delta V_{ISENSE}}{\Delta D_{OFF}} \times \frac{\Delta D_{OFF}}{\Delta I_{EAO}} \times \frac{\Delta I_{EAO}}{\Delta I_{Isense}} \quad (1)$$

$$\Delta V_{IEAO} = G_{MI} \times Z_{CI} \quad (2)$$

$$\frac{\Delta V_{R_{SENSE}}}{\Delta V_{I_{EAO}}} \equiv \frac{(b)}{(a)} \quad (3)$$

$$(b) \frac{(V_o - V_{IN})}{SL} \times R_{SENSE}$$

由 fig2 可知

$$\frac{V_{R_{TC_T P-P}}}{T_s} = \frac{\Delta V_{I_{EAO}}}{DT_s}, \Delta V_{I_{EAO}} = DV_{R_{TC_T P-P}} \quad (4)$$

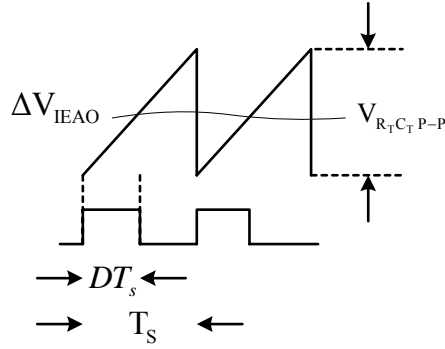


圖 2 ramp & $\Delta V_{I_{EAO}}$ 波形

將式(4)代入(3)可得

$$\frac{\Delta V_{R_{SENSE}}}{\Delta V_{I_{EAO}}} \equiv \frac{(b)}{(a)} = \frac{(V_o - V_{IN}) \times R_{SENSE}}{DV_{R_{TC_T P-P}}} \quad (5)$$

boost 電壓轉換比：

$$\frac{V_o}{V_{IN}} = \frac{1}{(1-D)} \quad (6)$$

式(6)代入式(5)可得

$$\frac{\Delta V_{R_{SENSE}}}{\Delta V_{I_{EAO}}} \equiv \frac{(b)}{(a)} = \frac{(V_o - V_{IN}) \times R_{SENSE}}{DV_{R_{TC_T P-P}}} = \frac{V_o \times R_{SENSE}}{SLV_{R_{TC_T P-P}}} = \frac{V_o \times R_{SENSE}}{\omega LV_{R_{TC_T P-P}}} \quad (7)$$

$$\text{set } \left| \frac{\Delta V_{R_{SENSE}}}{\Delta V_{I_{EAO}}} \right| = 1 \text{ 可求出 crossover frequency } \omega_c = \frac{V_o \times R_{SENSE}}{LV_{R_{TC_T P-P}}} \quad (8)$$

由式(8)可繪出其波德圖，其中 $\omega_p = \frac{2}{RC}$

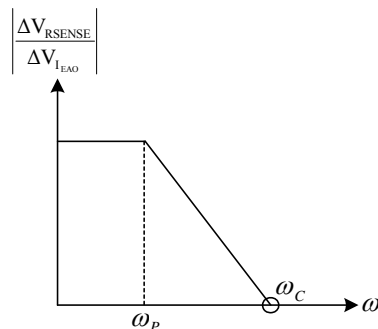


圖 3 $\left| \frac{\Delta V_{RSENSE}}{\Delta V_{I_{EAO}}} \right|$ 大小與頻率響應圖

(F)VEAO :

VEAO 的補償為 GM_v 乘上 zero-pole network，一般選擇其 unity-in(crossover-frequency) 為 $\frac{1}{2}$ line-frequency = 30Hz (或 25Hz)，zero 的位置為 0.1pole。

voltage loop show in fig1. As illustrated in fig.1 the loop gain can be written equation(1).

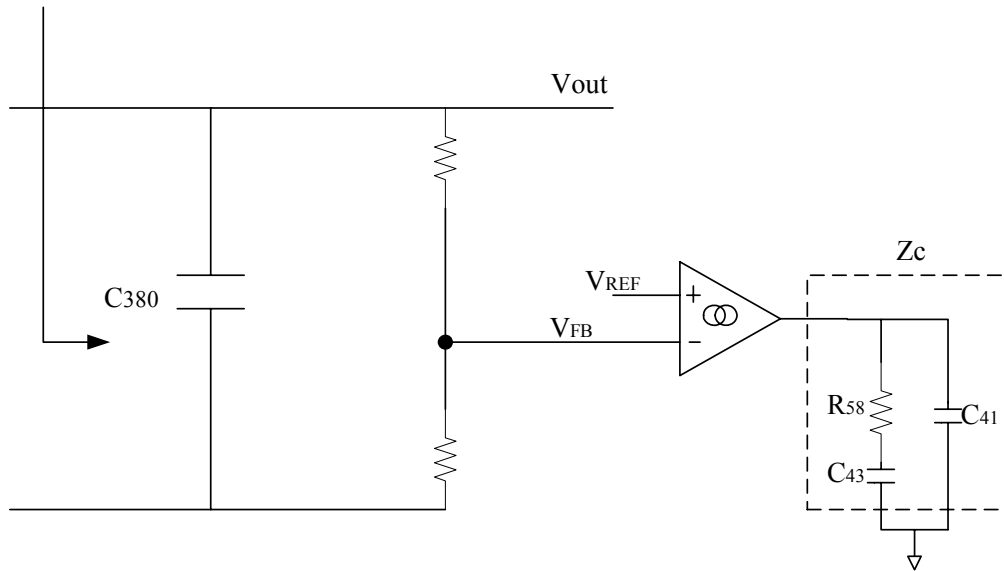


fig.1 voltage loop

$$\begin{aligned} \text{Loop gain of the voltage loop} &= \left(\frac{dV_{out}}{dV_{eao}} \right) \times \left(\frac{dV_{fb}}{dV_{out}} \right) \times \left(\frac{dV_{eao}}{dV_{fb}} \right) \\ &= \frac{P_{in} \times 2.5V \times GM_v \times Z_{CV}}{V_{out} \times \Delta V_{eao} \times S \times C_{380} \times V_{out}} \end{aligned} \quad (1)$$

note:

Pin: Max. input power

GM_v : VEAO's transconductance(90umho)

Z_{cv} : compensation Net Work at VEAO(voltage error amplifier)

V_{out} : PFC boost converter output voltage

D_{veao} : Max. effective swing which is 6V-.625V=5.375V(IC internal)

set unity gain frequency at 25Hz, from equation (1) we can obtain equation (2).

$$1 = \frac{P_{in} \times 2.5V \times GM_v \times Z_{CV}}{V_{out} \times \Delta V_{eao} \times S \times C_{380} \times V_{out}}, \text{ at } 25\text{Hz} \quad (2)$$

using equation (2), we can find $GM_v \times Z_{cv}$

$$GM_V \times Z_{CV} = \frac{V_{out} \times \Delta V_{eao} \times S \times C_{380} \times V_{out}}{Pin \times 2.5}$$

$$= \frac{390V \times 5.375V \times S \times 150\mu F \times 390}{Pin \times 2.5} \approx GM_V \times R_{58} \quad (3)$$

note:

$V_{out}=390V$

$C_{380} = 150\mu F$

$GM_V \approx 90 \mu mho$

Set $P_{out}=240Watt$, $efficiency=70\%$, $\therefore Pin = 342Watt$

Using equation (3), R_{58} is

$$R_{58} = 162K\Omega \quad at GM_V = 90 \mu mho$$

using unity gain frequency at $7Hz (f_c)$, $f_c = 7 HZ \approx \frac{1}{2 \times \pi \times R_{58} \times C_{41}}$, therefore

$R_{58} = 162K\Omega$, $C_{41} = 140nF$, $R_{58} = 124K\Omega$, $C_{41} = 183.358nF$. Let the zero $=0.1$ pole, therefore, $f_z = 0.7 HZ$ and

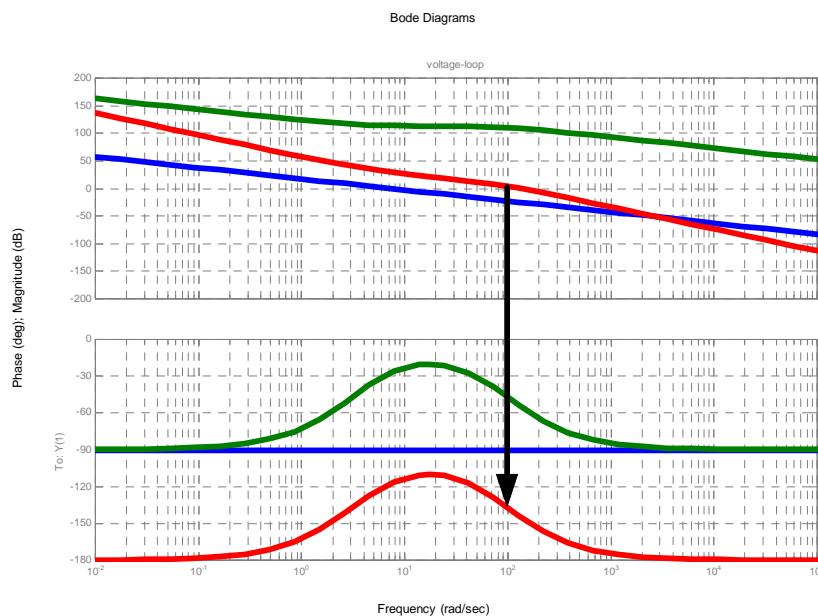
$C_{43} = 10 C_{41}$, $R_{63} = 475K\Omega$, $C_{56} = 0.47\mu F$, $C_{57} = 0.022\mu F$

$$pole = \frac{1}{2 \times \pi \times R_{63} \times C_{56}} = 3.28 H_z, \quad zero = \frac{1}{2 \times \pi \times R_{63} \times C_{57}} = 0.328 H_z$$

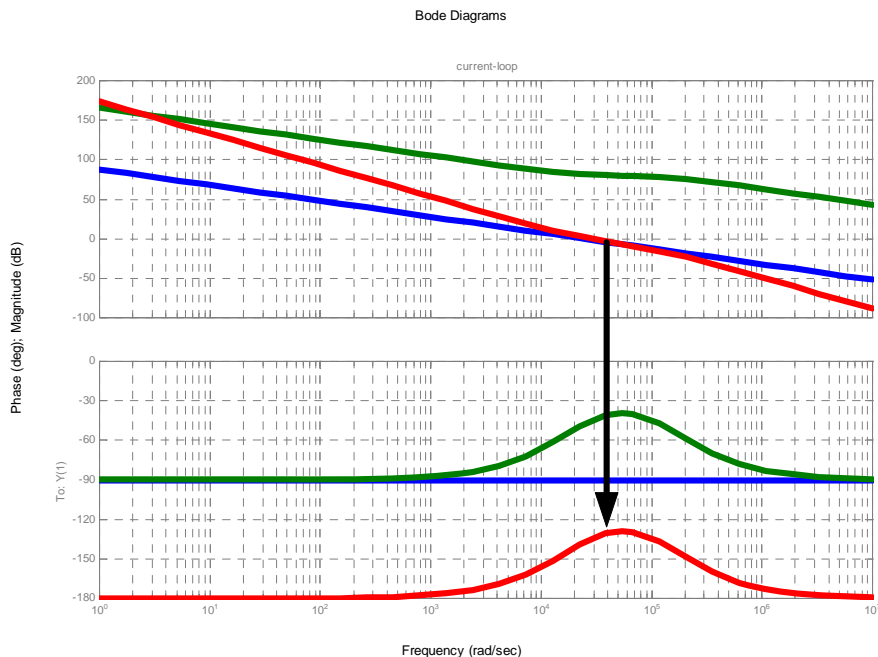
Example : $P_{out}=240W$, $\eta = 0.7$, PFC choke= $800\mu H$, bulk cap.= $150\mu F$, $R_{sense}=0.1 \Omega // 0.15 \Omega$

bulk cap voltage= $380(V_{eao}:R=475K+C1=684P//C2=223P)$

voltage-loop



current-loop (I_{ea}:R=11K+C1=472P//C2=681P)



Test conditions:

The loop stability is measured at the minimum and maximum AC line, and both at minimum and maximum load.

Pass/Fail criteria:

Phase margin has to be greater than 45deg. Data must be provided by the Power Supply vendor.

Test Result:

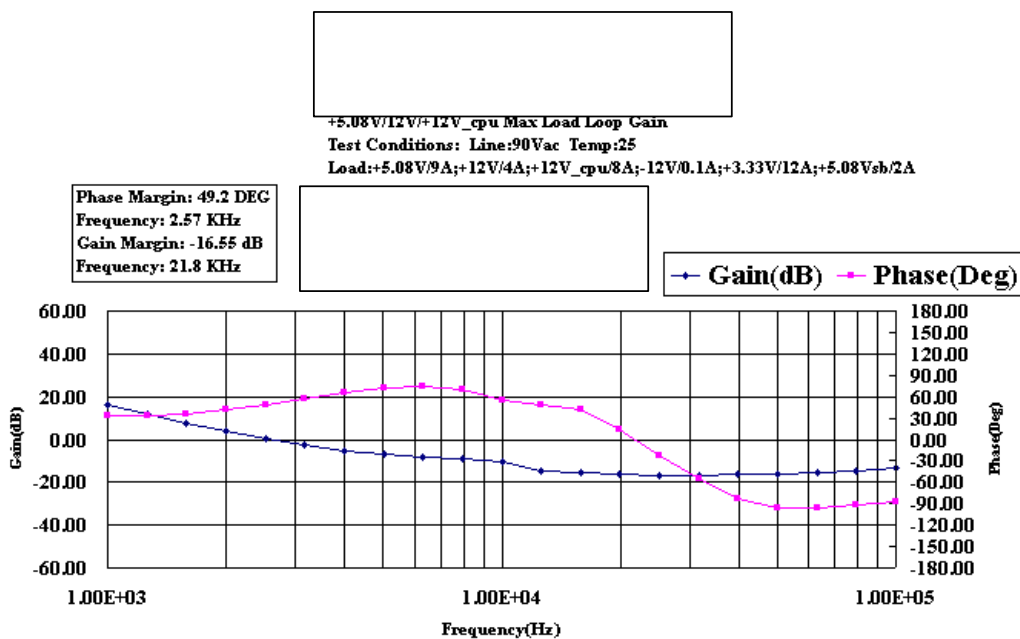
Pass

The worse case is

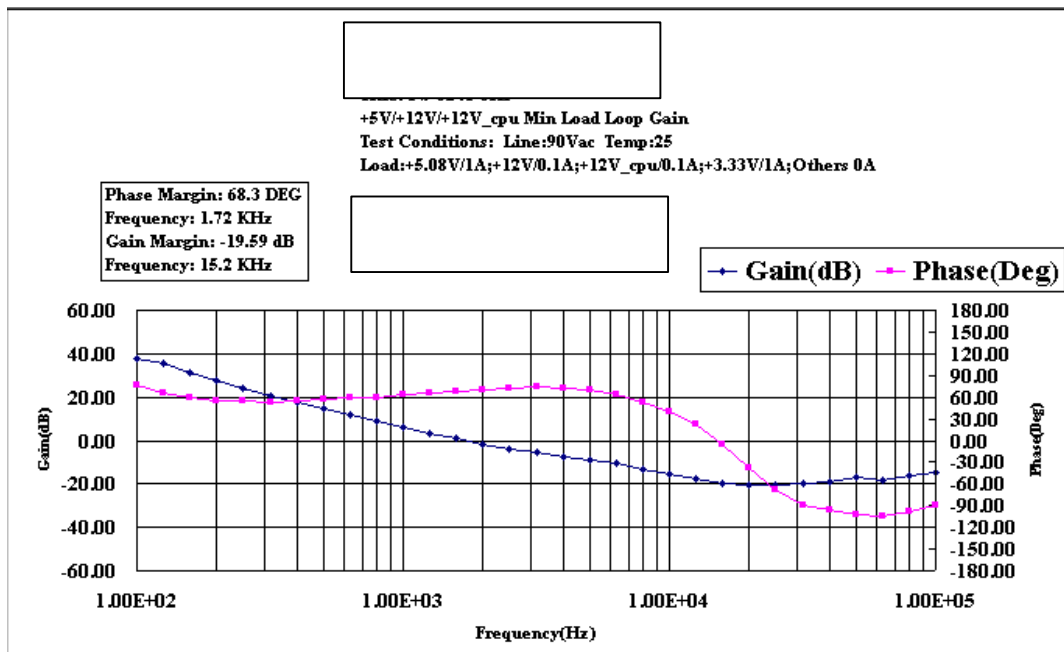
Phase margin : 48.3° at 264V/50Hz max. load

Gain margin : -15.46 dB at 264V/50Hz max. load

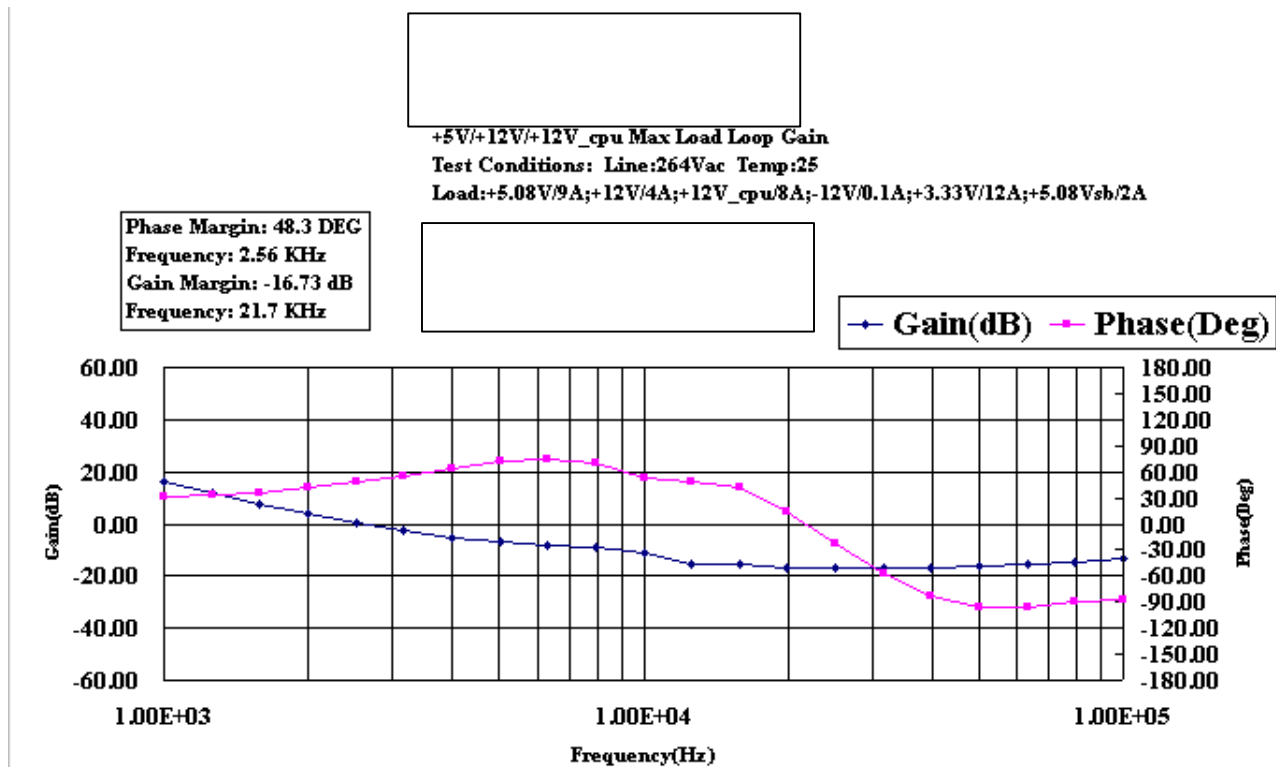
90Vac Max. Load (+5.08V/+12V/+12V_cpu Loop Gain)



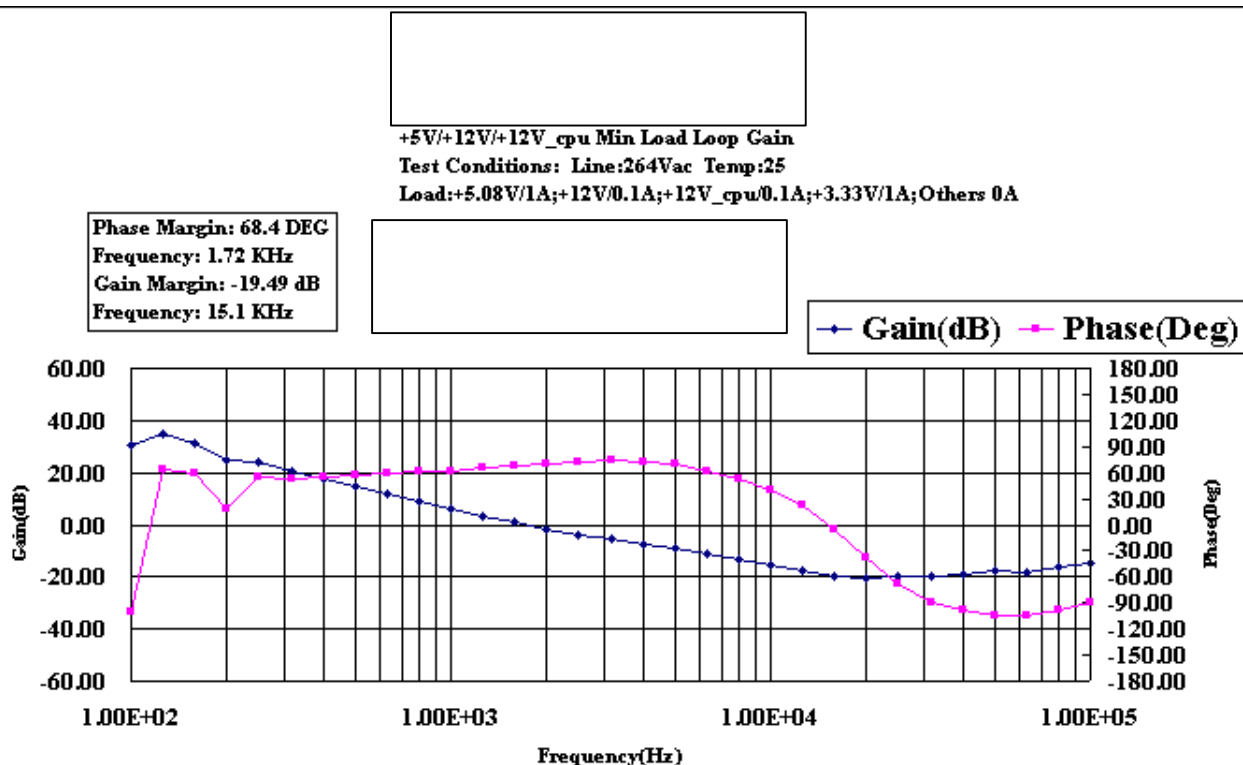
90Vac Min. Load (+5.08V/+12V/+12V_cpu Loop Gain)



264Vac Max. Load (+5.08V/+12V/+12V_cpu Loop Gain)



264Vac Min. Load (+5.08V/+12V/+12V_cpu Loop Gain)



AC 如何轉換成 DC

交流電壓如何轉換至直流電壓，如圖 1，在橋式整流輸入端與輸出端之間加入電力轉換器 (converter)，同時可達到功因校正與輸出直流電壓的功能。

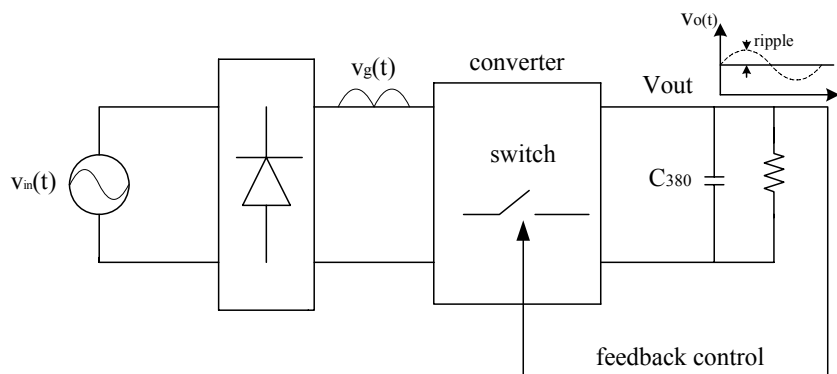


圖 1 AC to DC 方塊圖

在分析前先所需了解兩點，(a) $p_{in}(t) \neq p_{out}(t)$ 輸入瞬時功率不等於輸出瞬時功率，(b) $\langle p_{in}(t) \rangle = \langle p_{out}(t) \rangle$ 輸入平均功率等於輸出平均功率 (note: 符號 $\langle \rangle$ ，表平均之意)。

法(1)：

$$W_{C_{380}} = \frac{1}{2} C v_c(t)^2 \quad (1)$$

$$P_{C_{380}} = \frac{d}{d_t} \left[\frac{1}{2} C v_c(t)^2 \right] = P_{in}(t) - P_R(t) \quad (2)$$

$$\begin{aligned} P_{in}(t) &= \frac{d}{d_t} \left[\frac{1}{2} C_{380} v_c(t)^2 \right] + P_R(t) = \frac{d}{d_t} \left[\frac{1}{2} C_{380} v_c(t)^2 \right] + \frac{v_c(t)^2}{R} \\ &= \frac{d}{d_t} \left[\frac{1}{2} C_{380} v_c(t)^2 \right] + \frac{2}{RC} \frac{1}{2} C_{380} v_c(t)^2 \end{aligned} \quad (3)$$

將式(3)取 Laplace 可得

$$P_{in}(S) = \left[S + \frac{2}{RC} \right] \left[\frac{1}{2} C v_c(t)^2 \right] \quad (4)$$

式(4)可表示成圖 2

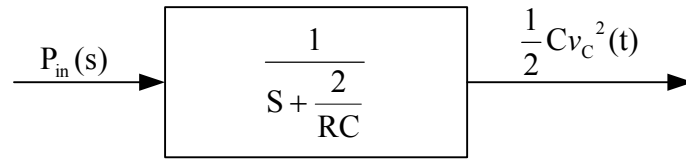


圖 2 AC to DC 轉移函數方塊圖

set $v_{in}(t) = V_M \sin \omega t$, $i_{in}(t) = I_M \sin \omega t$, V_M/I_M : 輸入電壓峰值/輸入電流峰值, 輸入功瞬時功率可表示成

$$P_{in}(t) = V_M I_M \sin^2 \omega t = \frac{V_M I_M}{2} (1 - \cos 2\omega t) \quad (5)$$

式(5)以波德圖可表示成圖 3, 由圖 3 中可看出, 若要輸出電壓漣波小, 則 $\frac{2}{RC} \ll 2\omega t$, 輸出電壓可獲得一個較好的直流電壓。

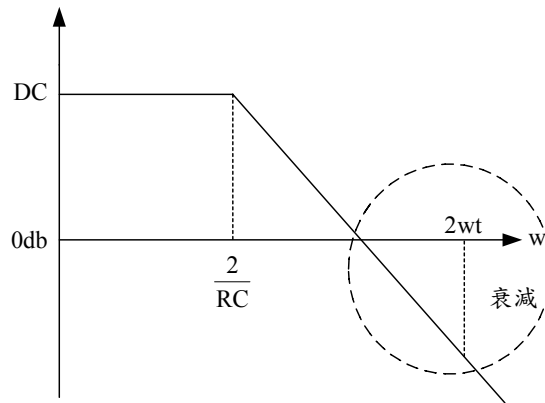


圖 3 輸入到輸出之 bode plot